

2/69

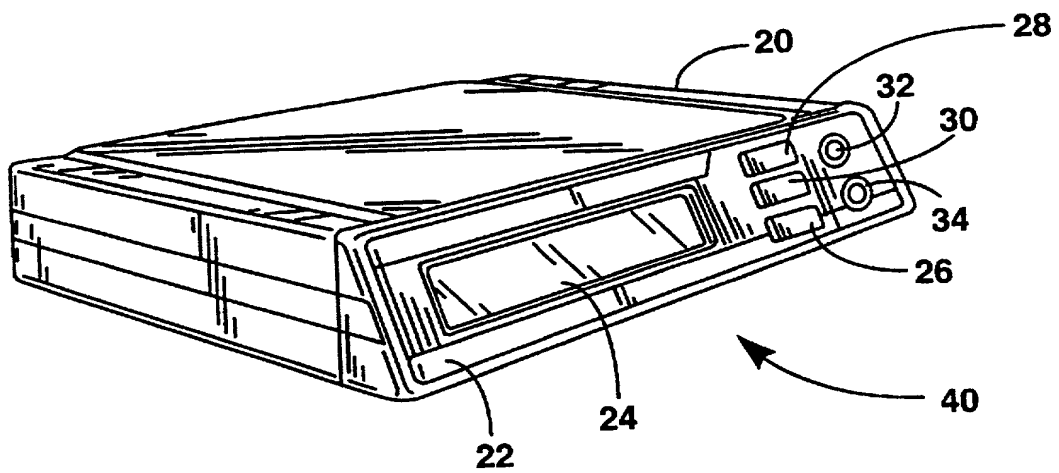


FIG. 2

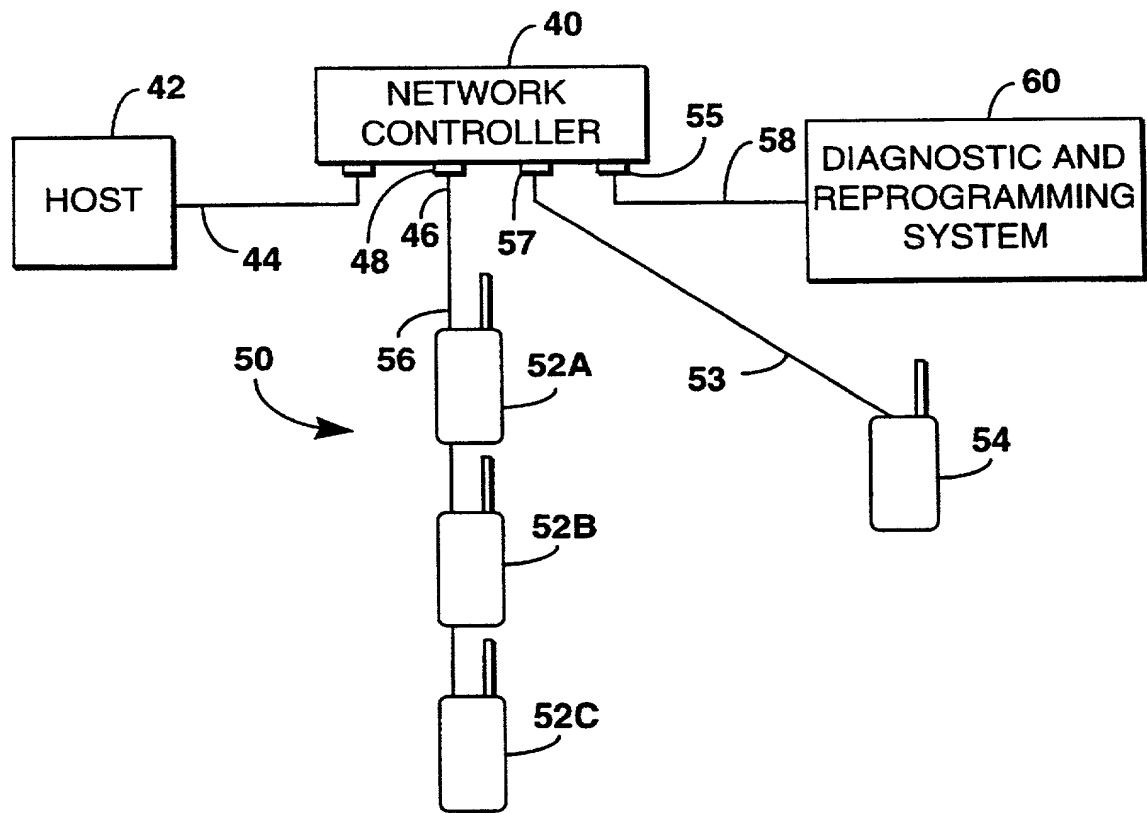


FIG. 3

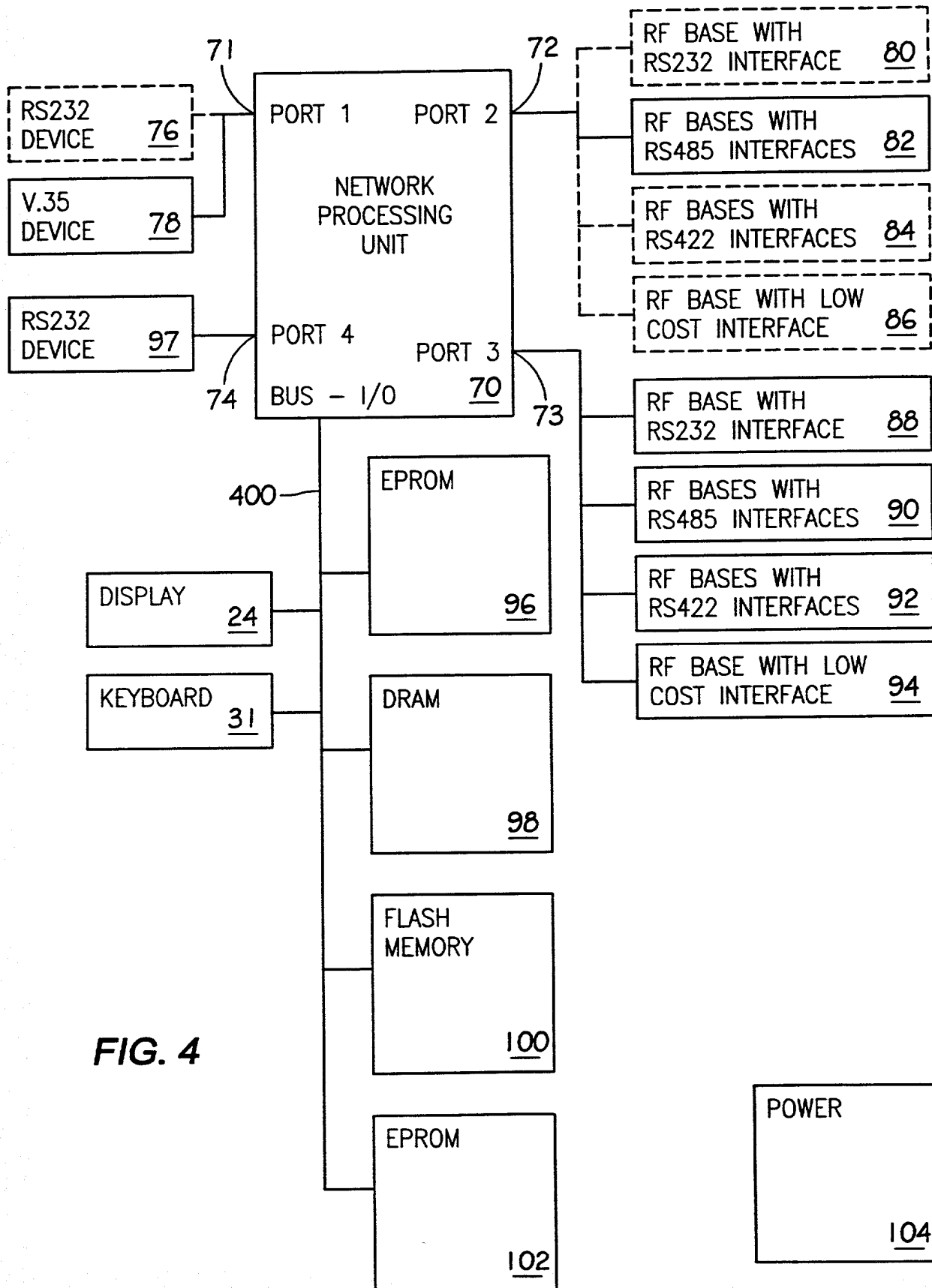
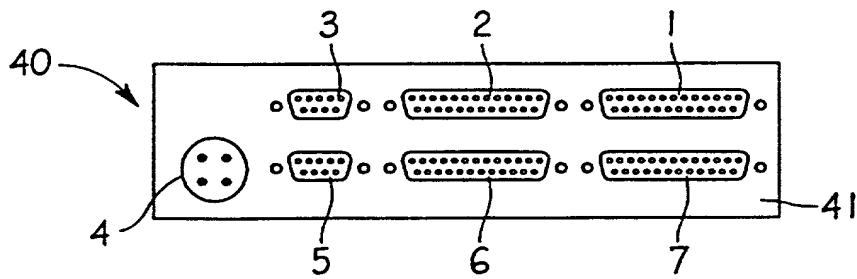


FIG. 4

**FIG. 5**

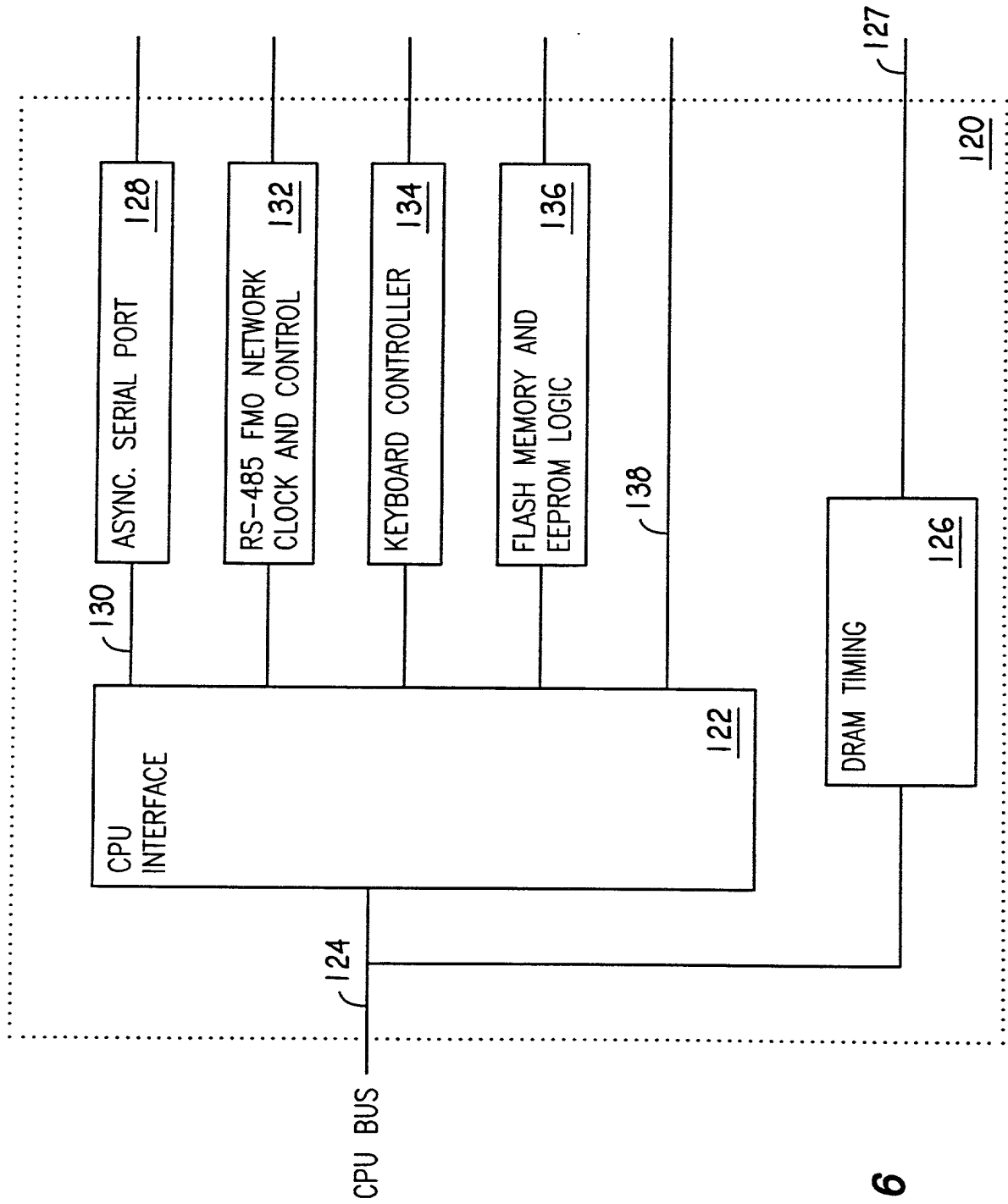
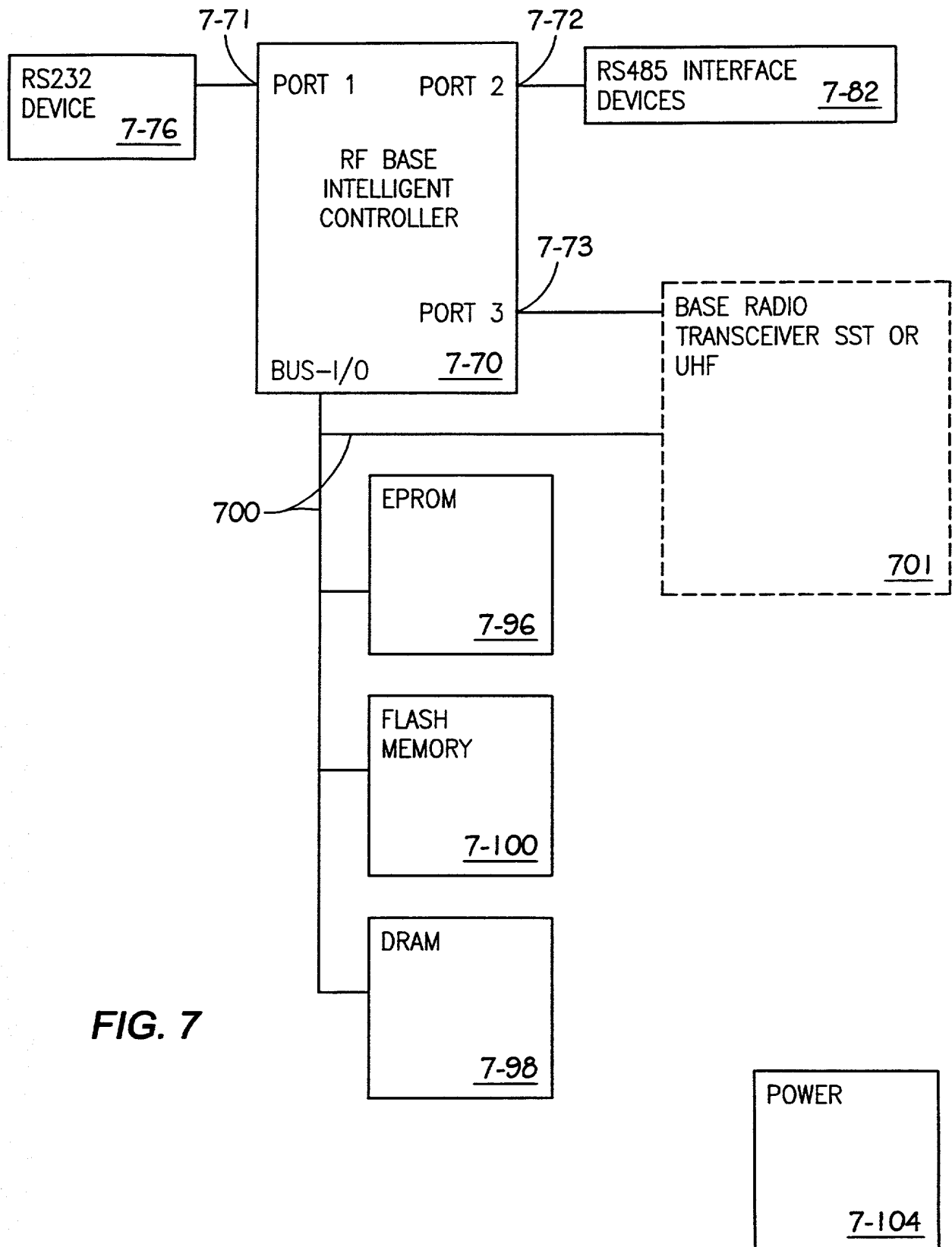


FIG. 6

7/69







9/69

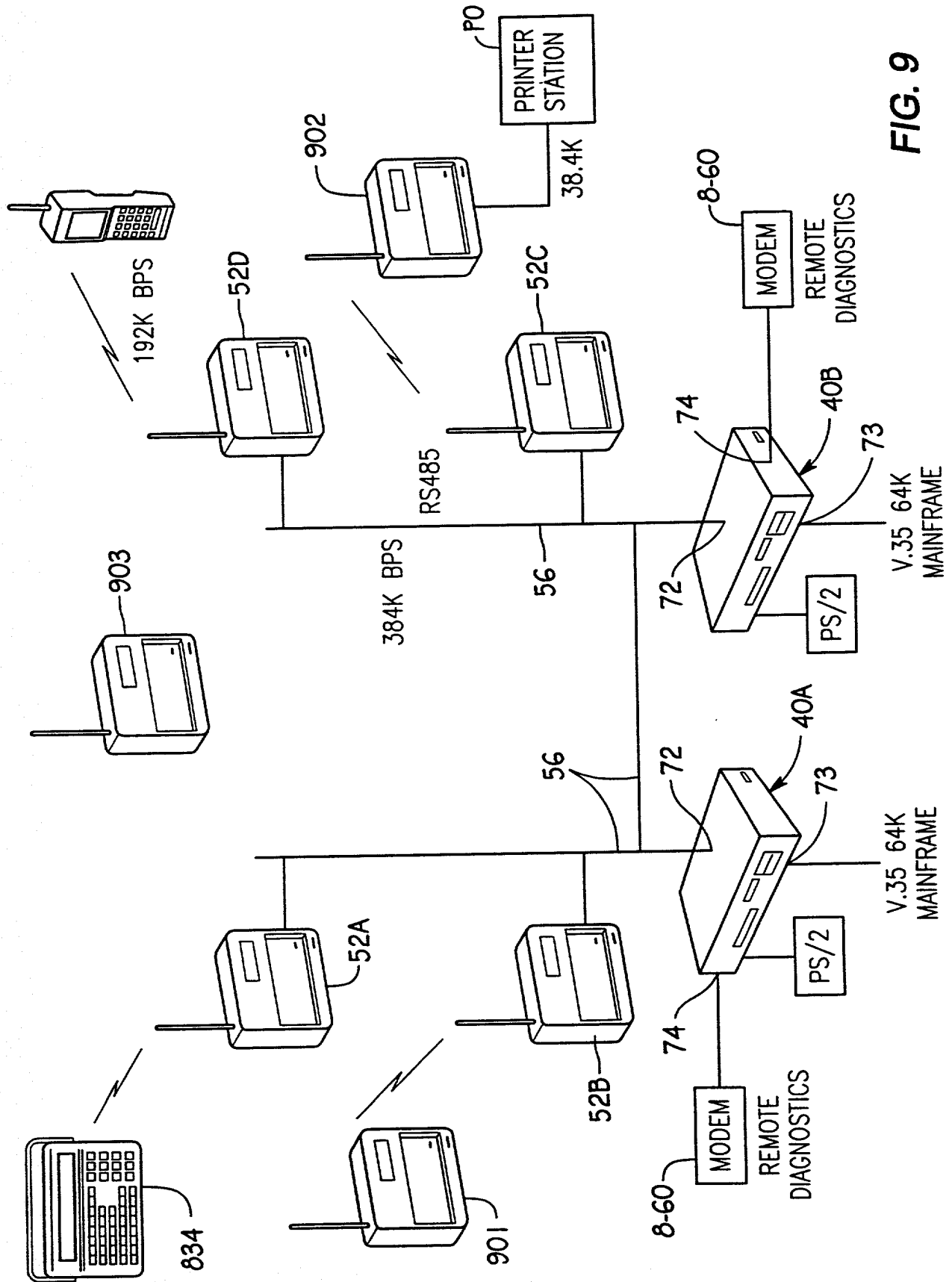


FIG. 9

10/69

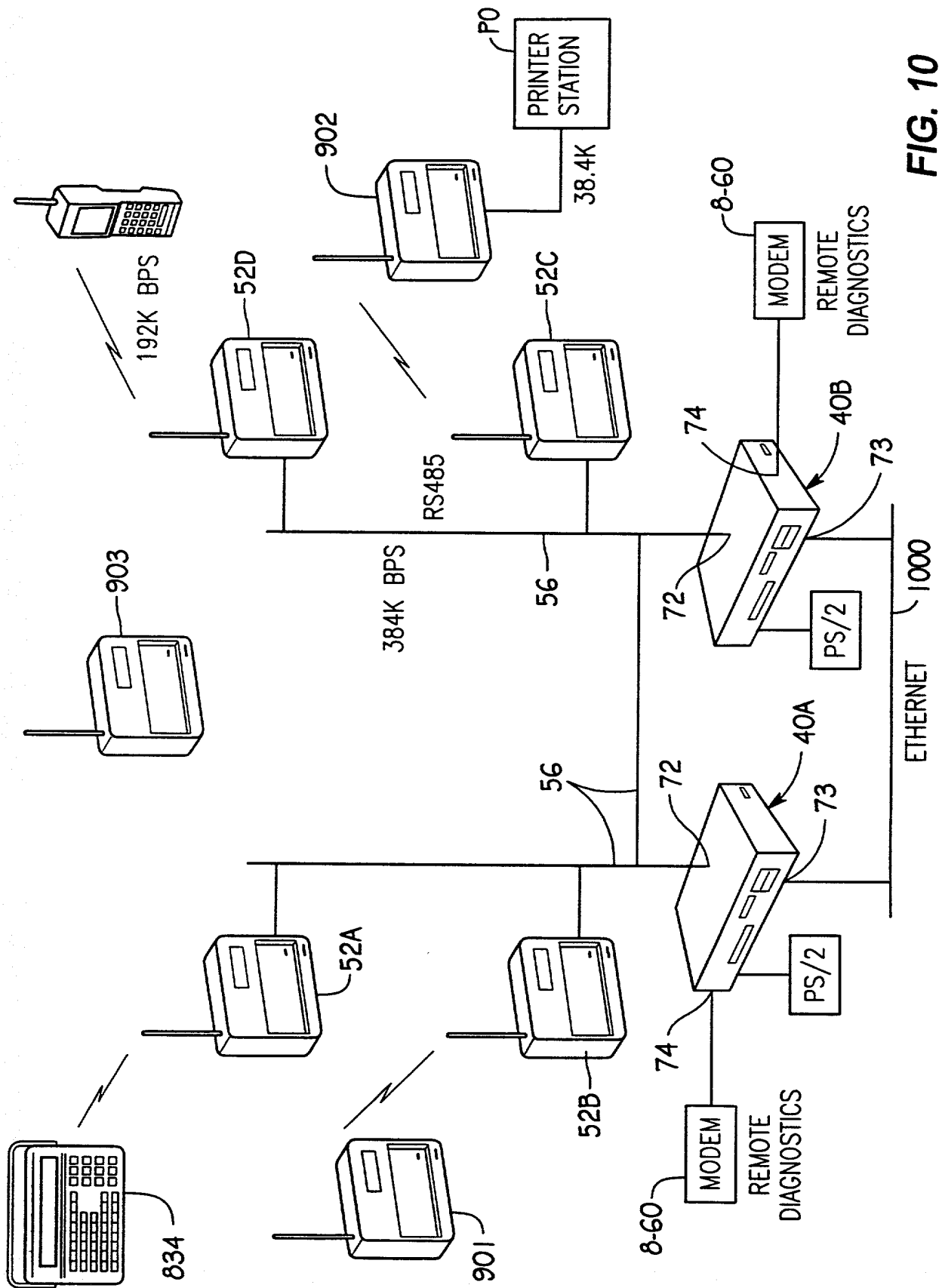


FIG. 10

11/69

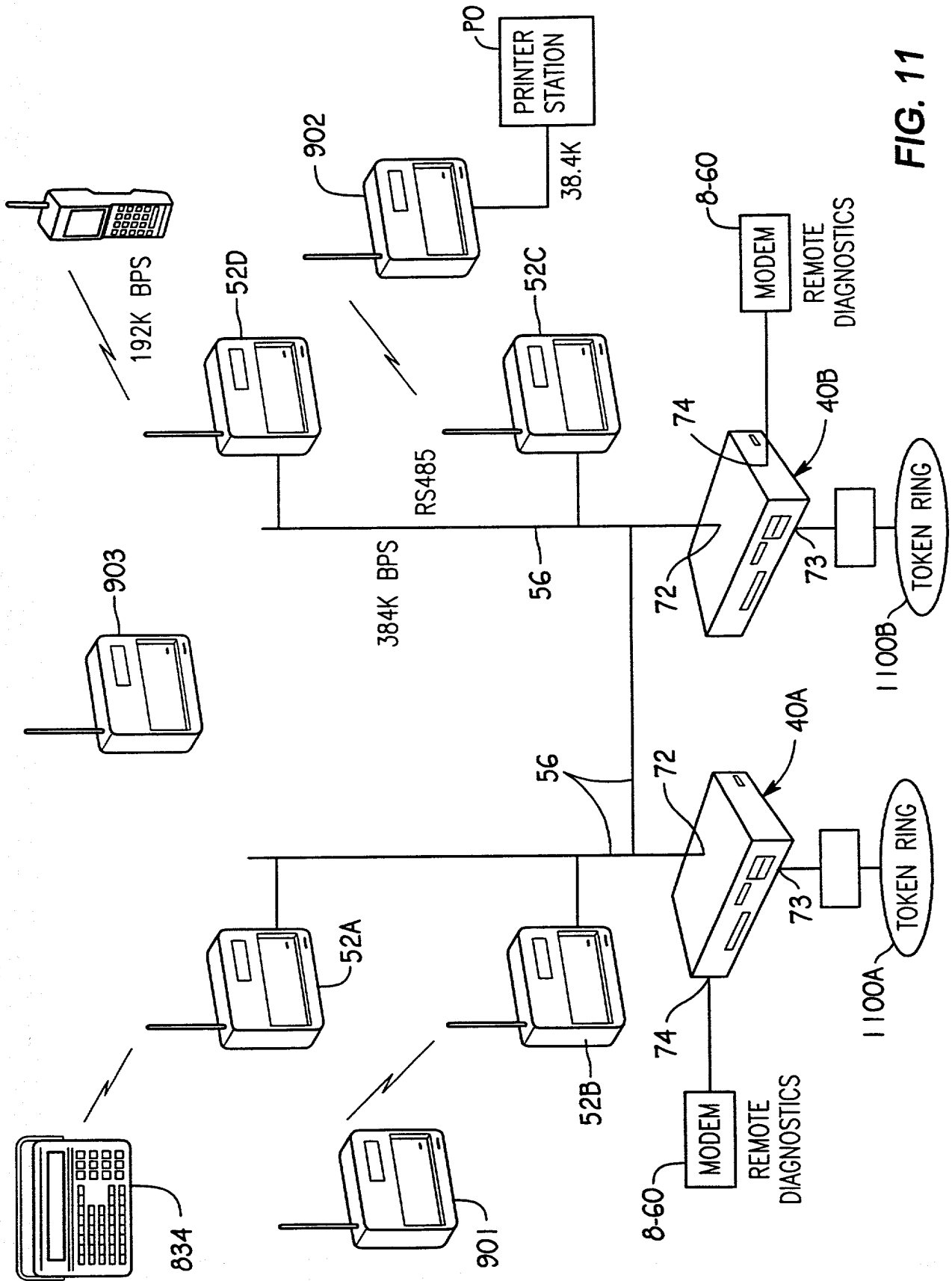


FIG. 11

12/69

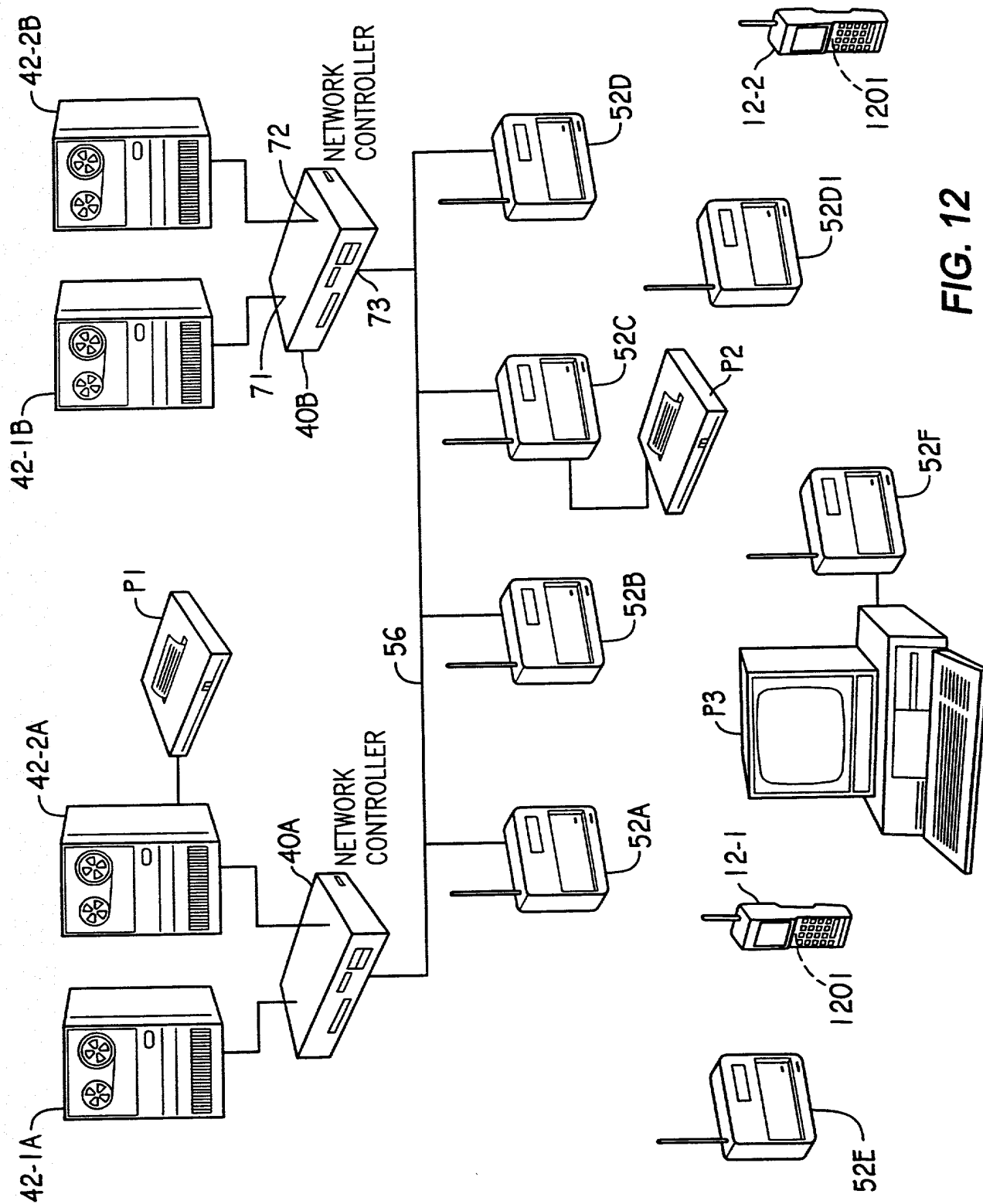


FIG. 12

13/69

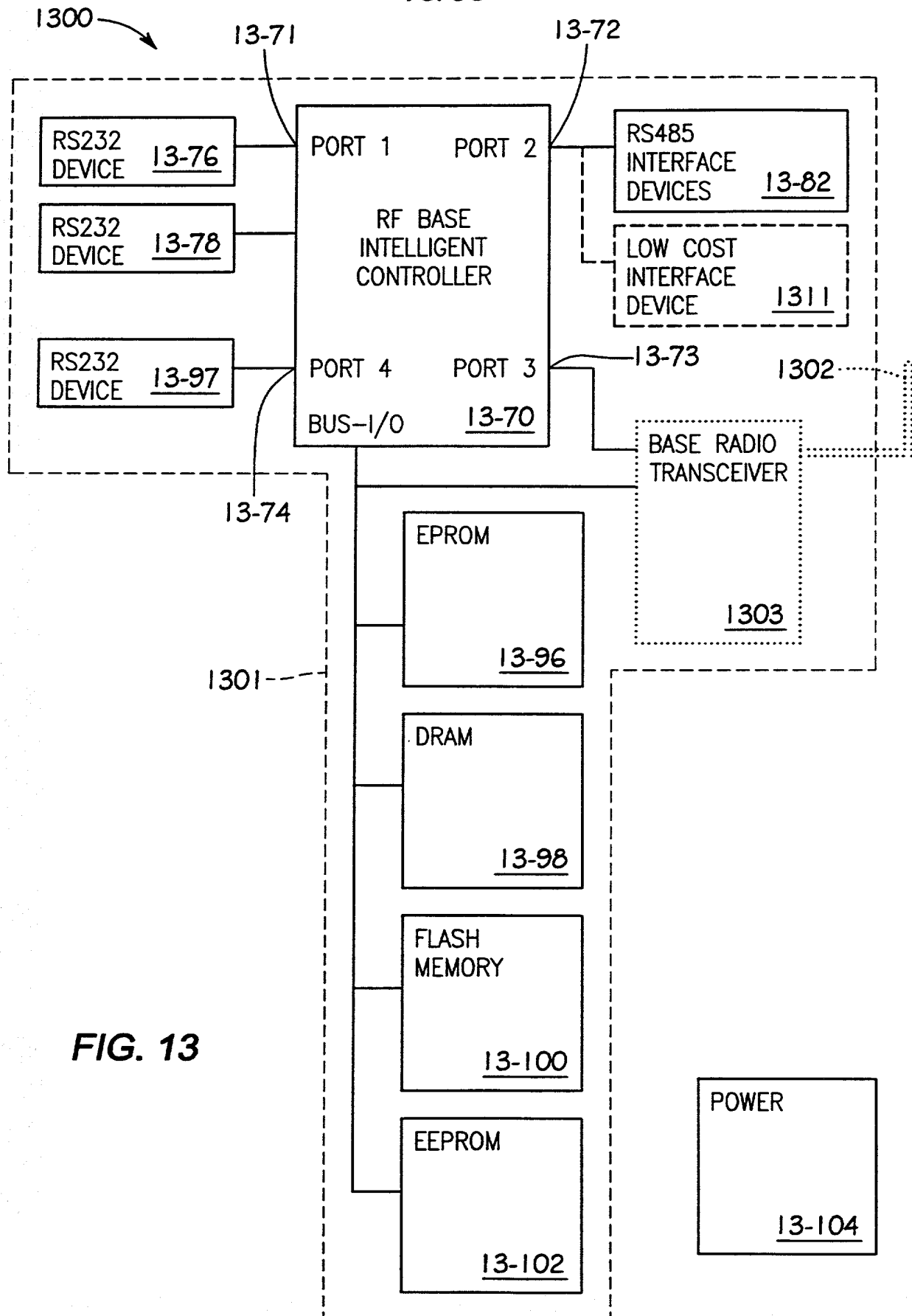


FIG. 13

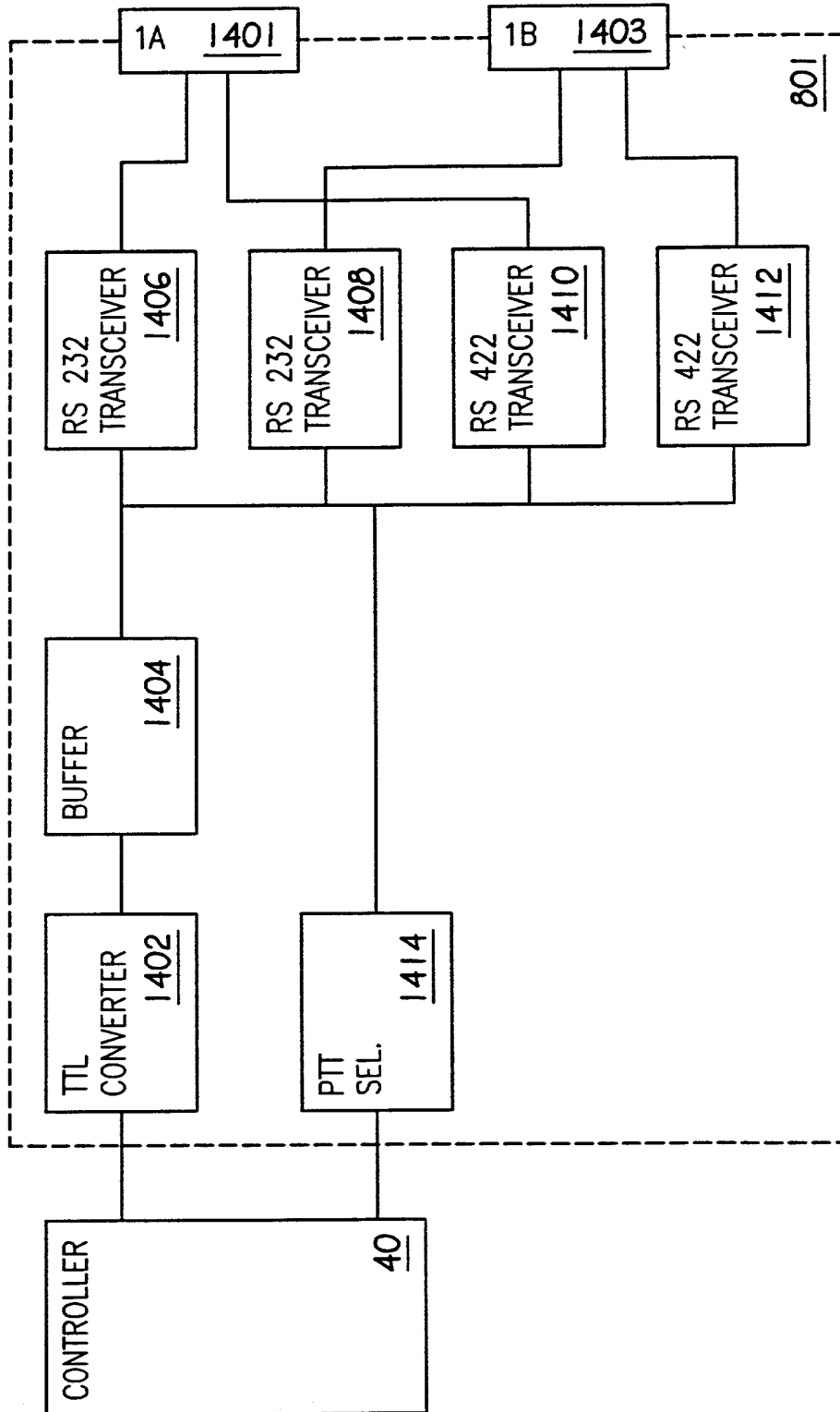


FIG. 14

15/69

MBA3000 MULTIPLE BASE ADAPTER

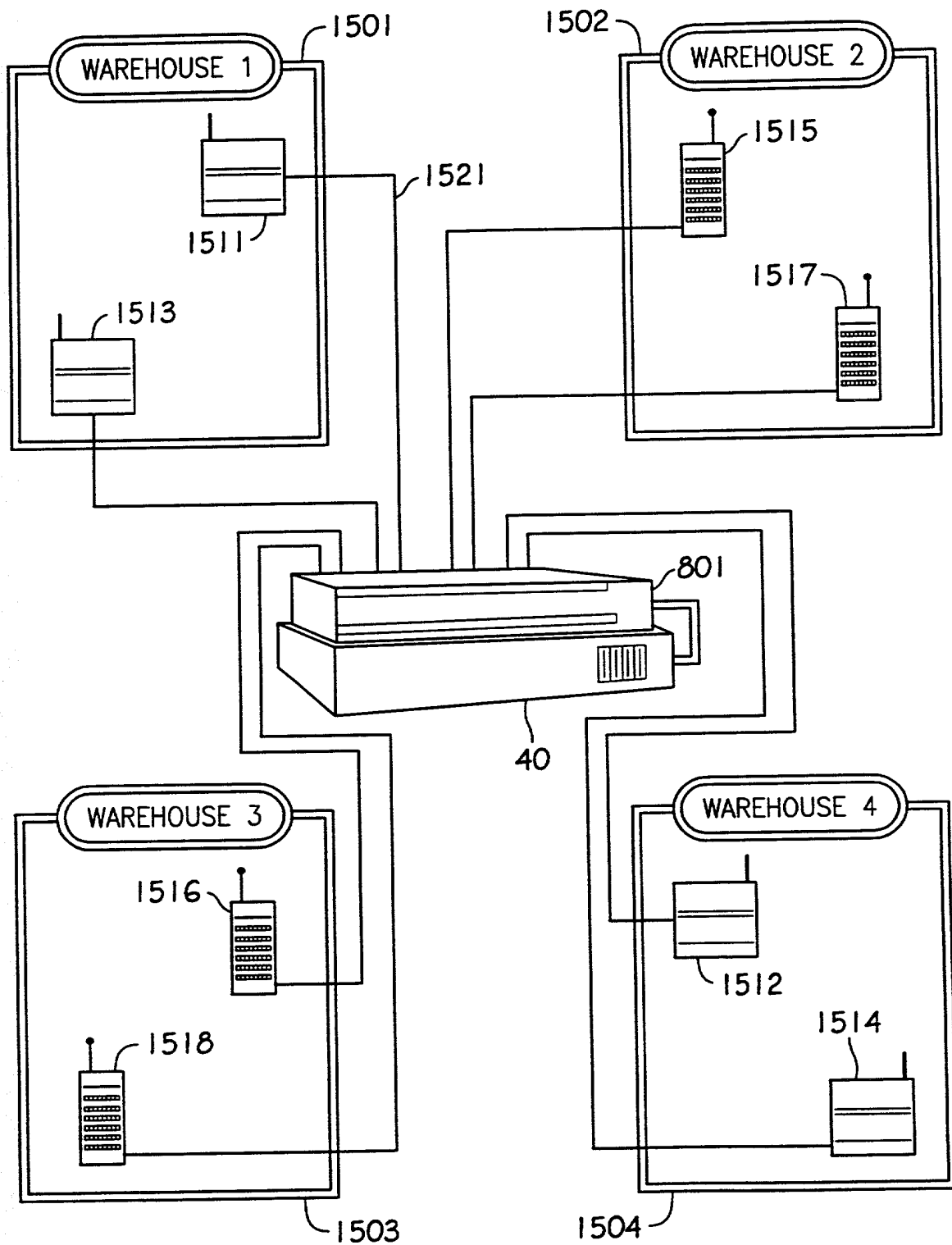


FIG. 15

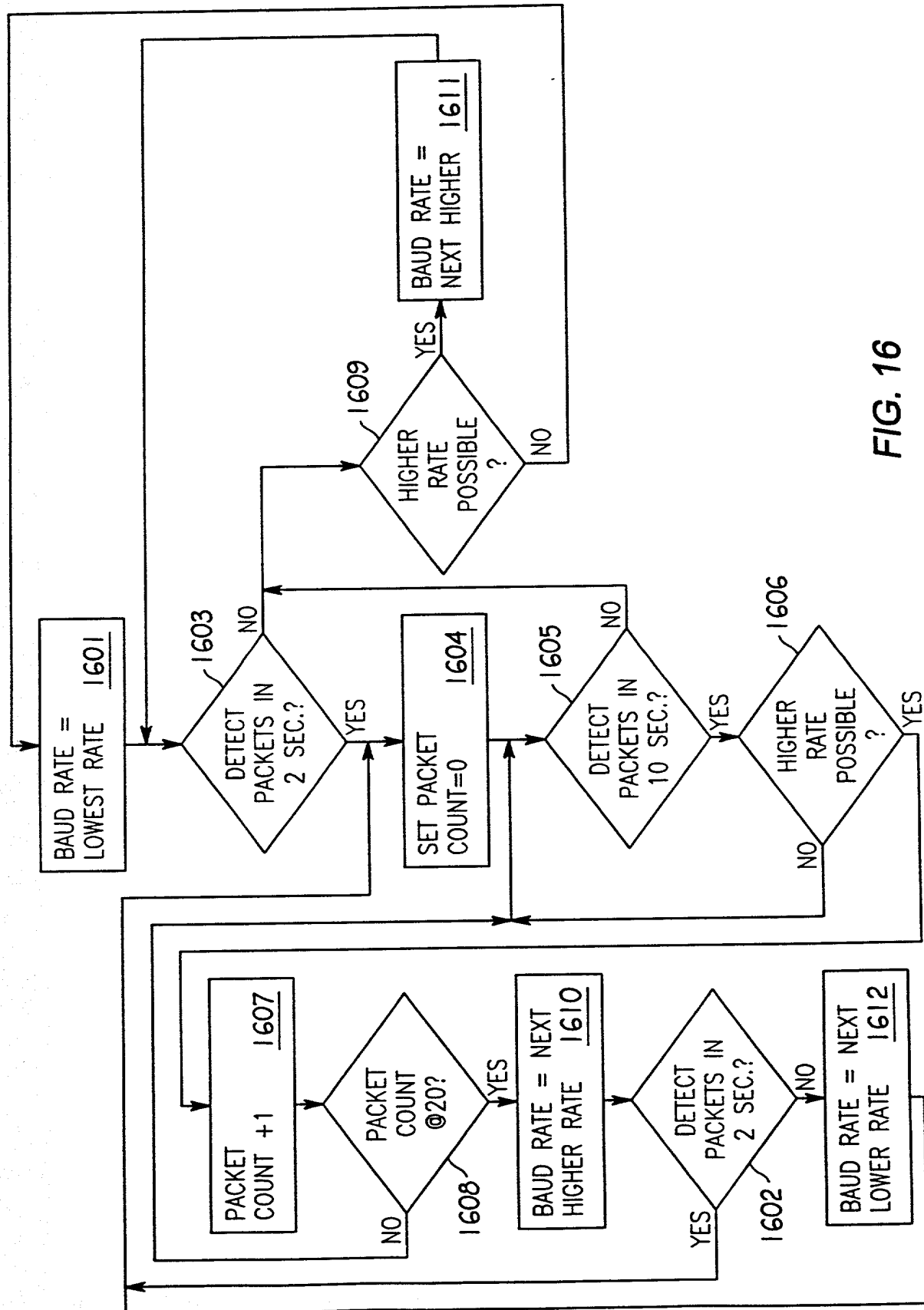


FIG. 16



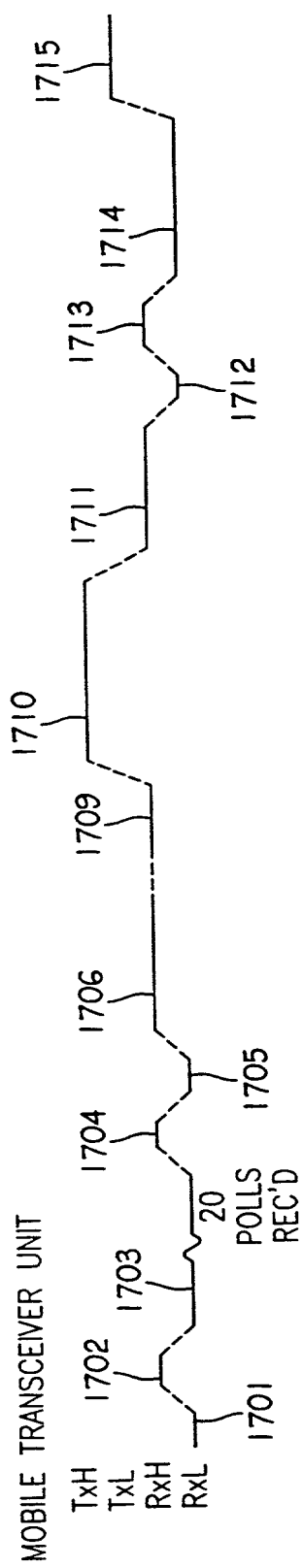


FIG. 17

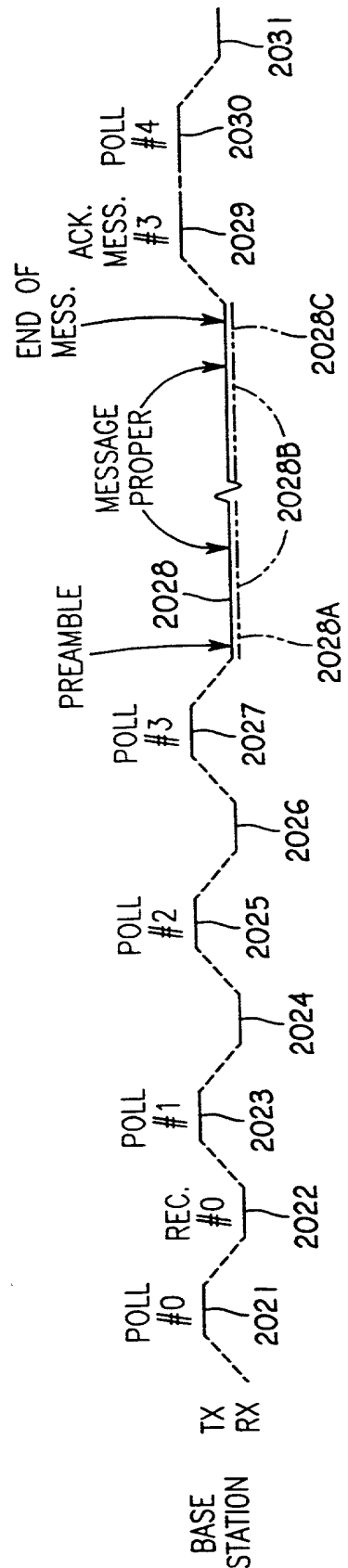


FIG. 18

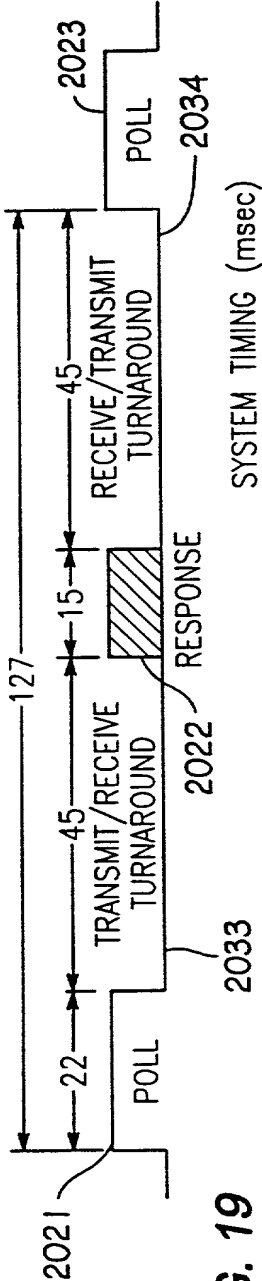


FIG. 19  
(PRIOR ART)

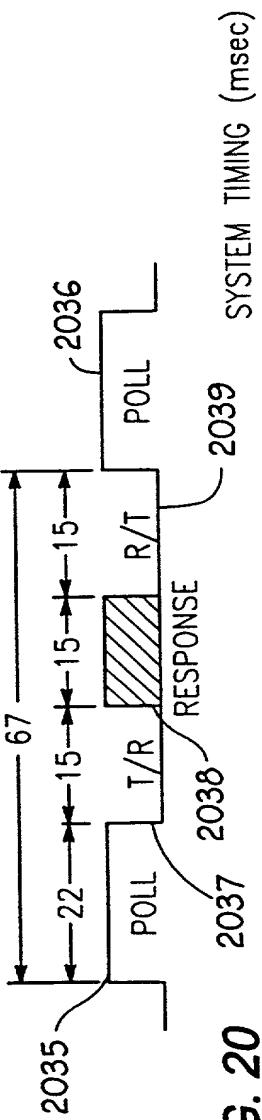


FIG. 20  
(PRIOR ART)

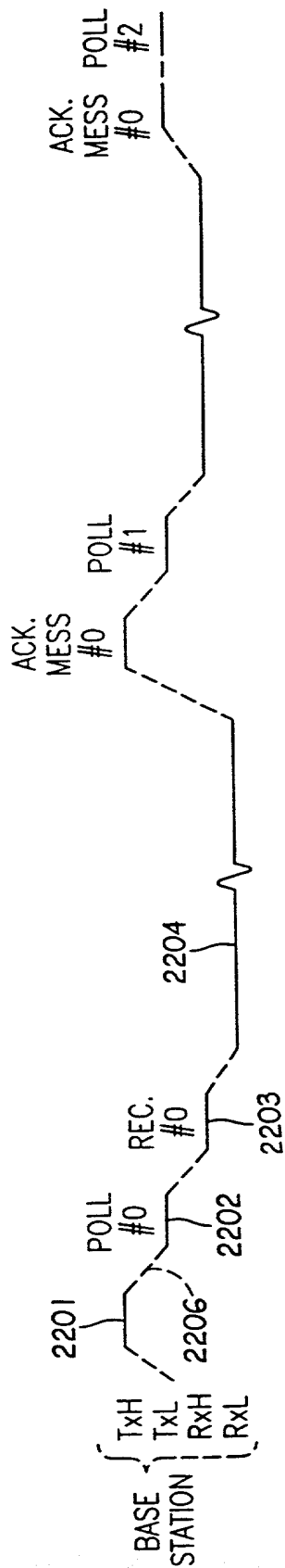


FIG. 33

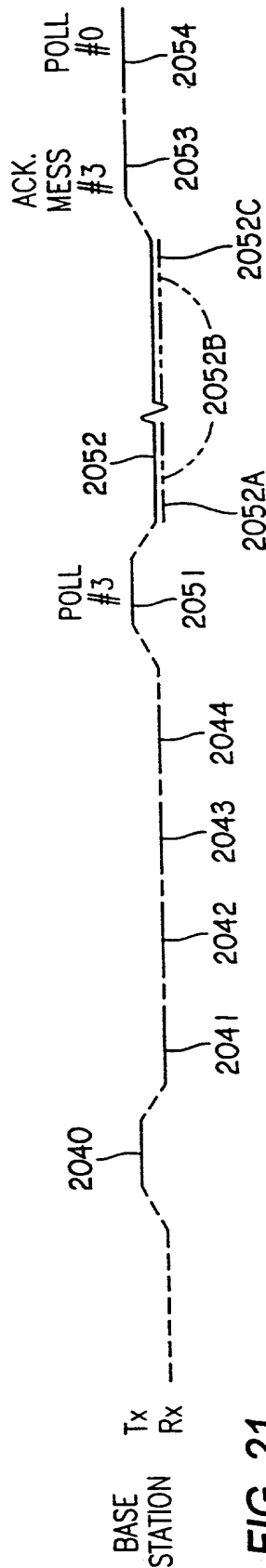


FIG. 21

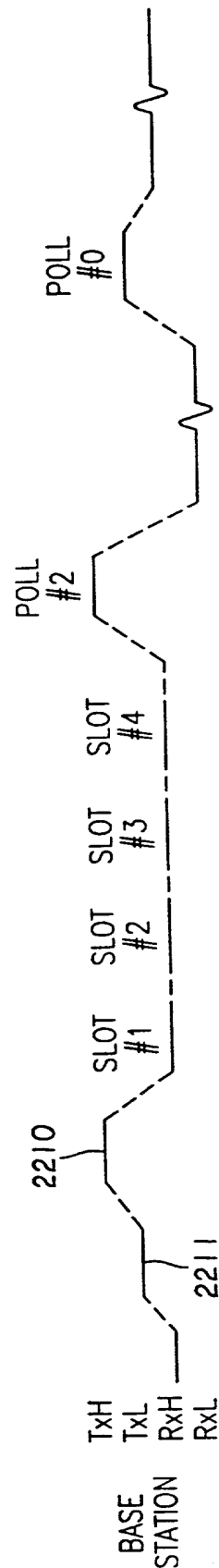


FIG. 34

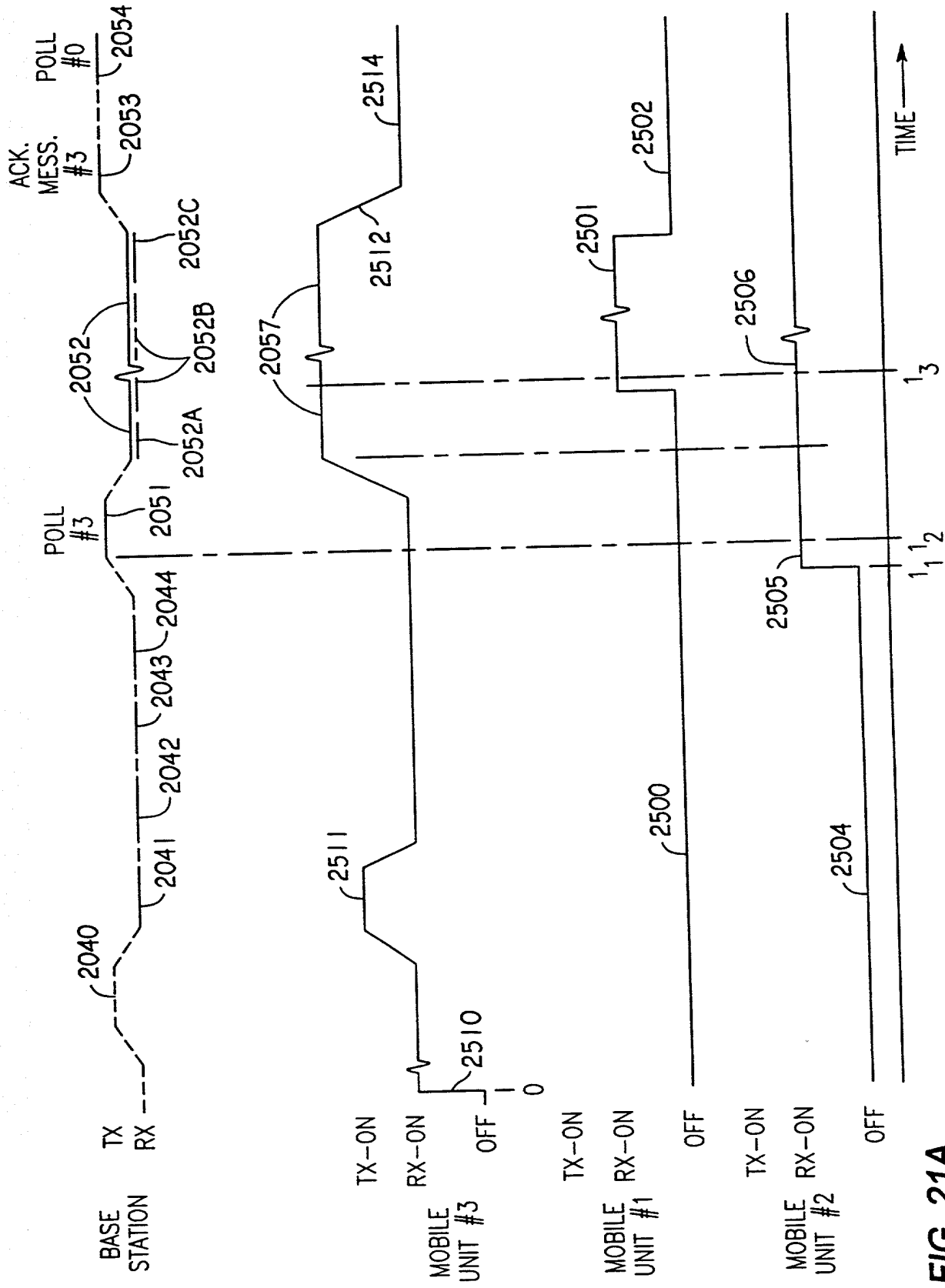


FIG. 21A

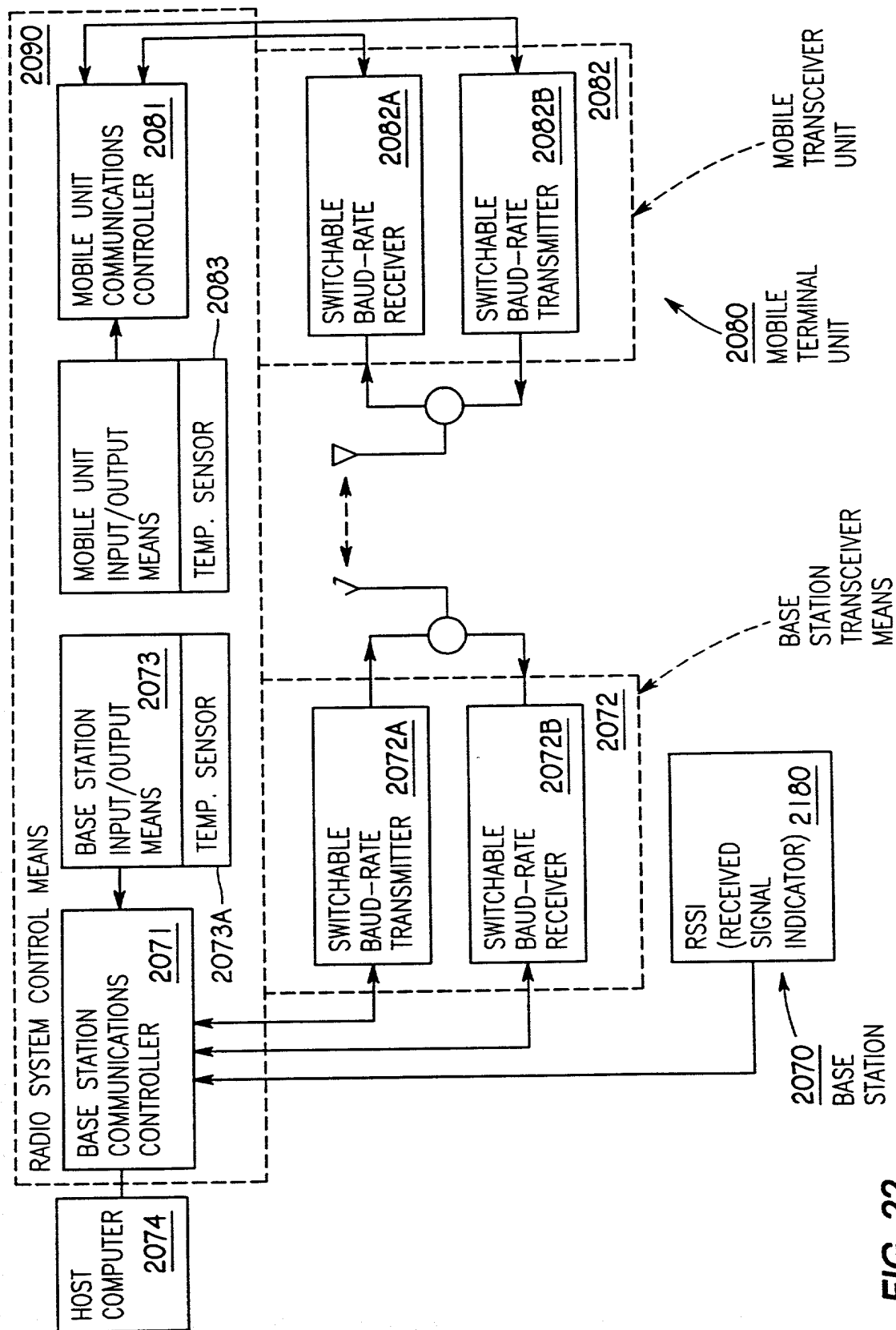
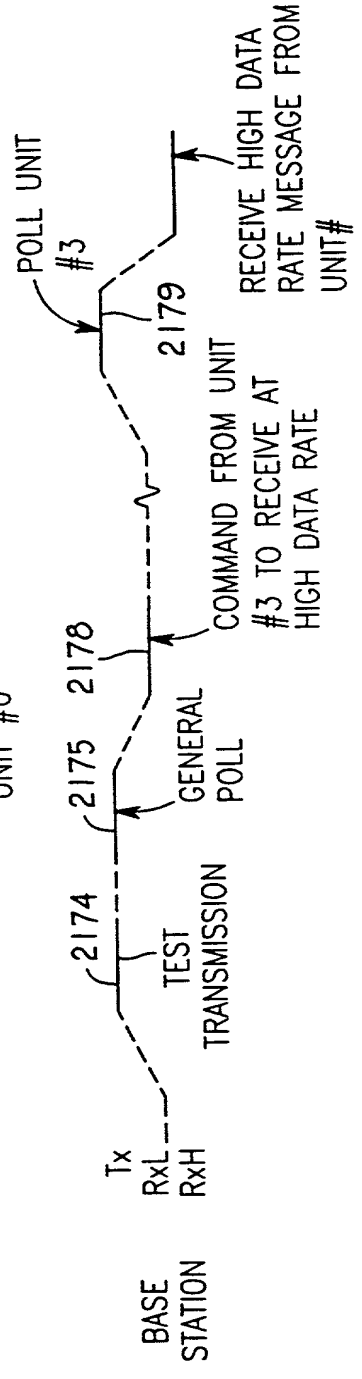
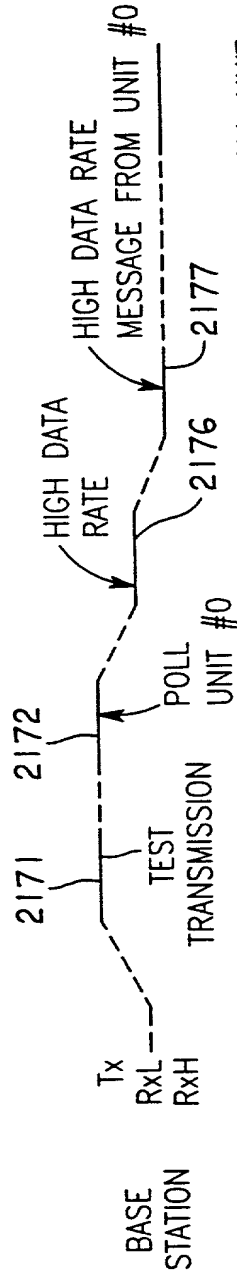
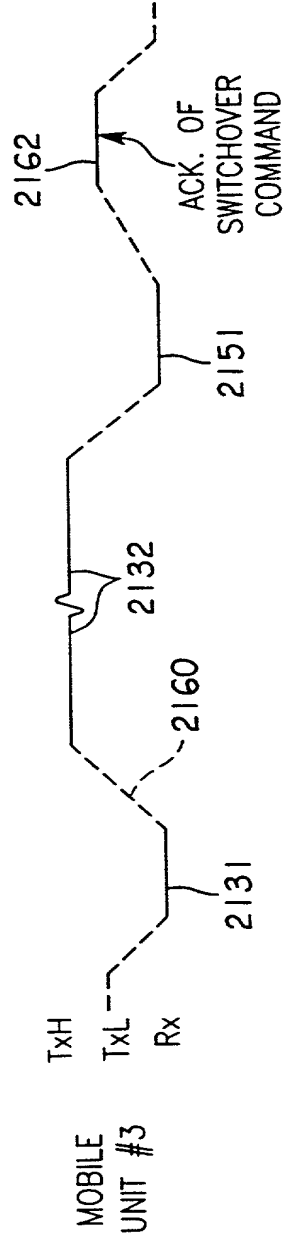
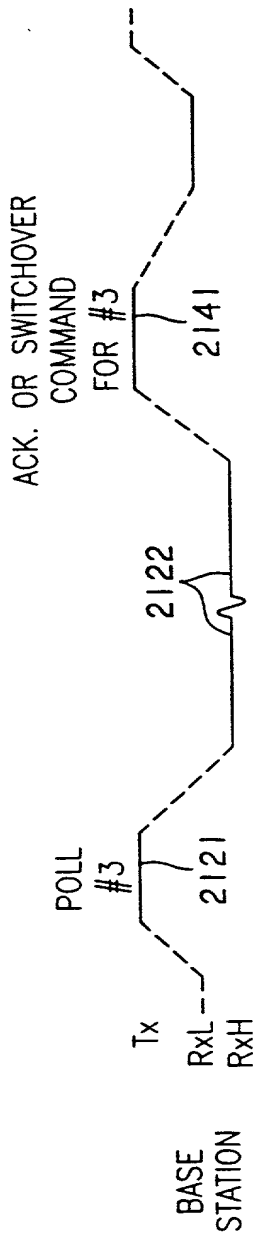


FIG. 22



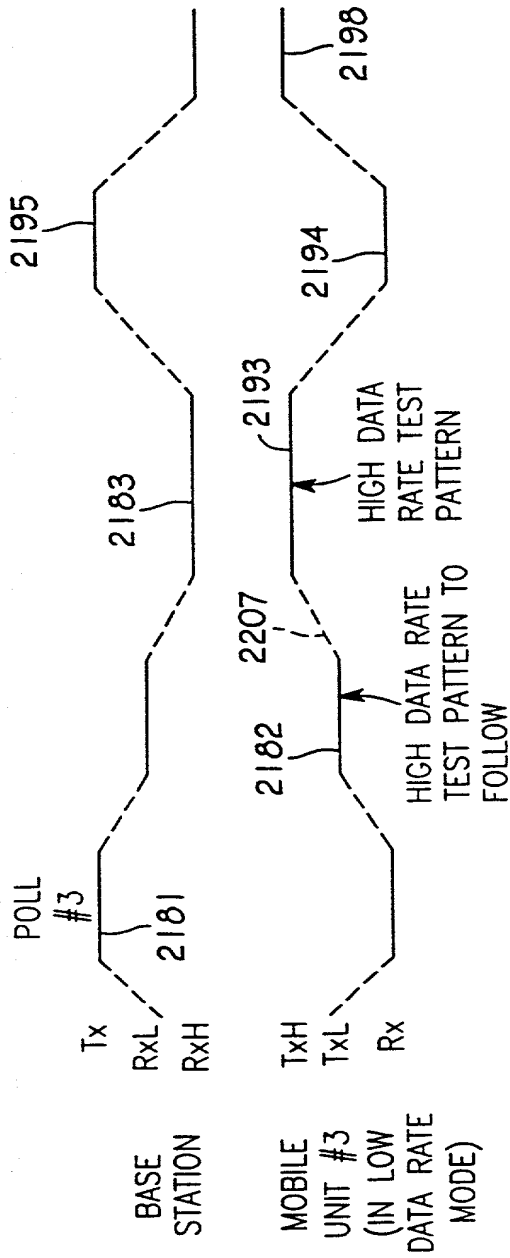


FIG. 31

FIG. 32

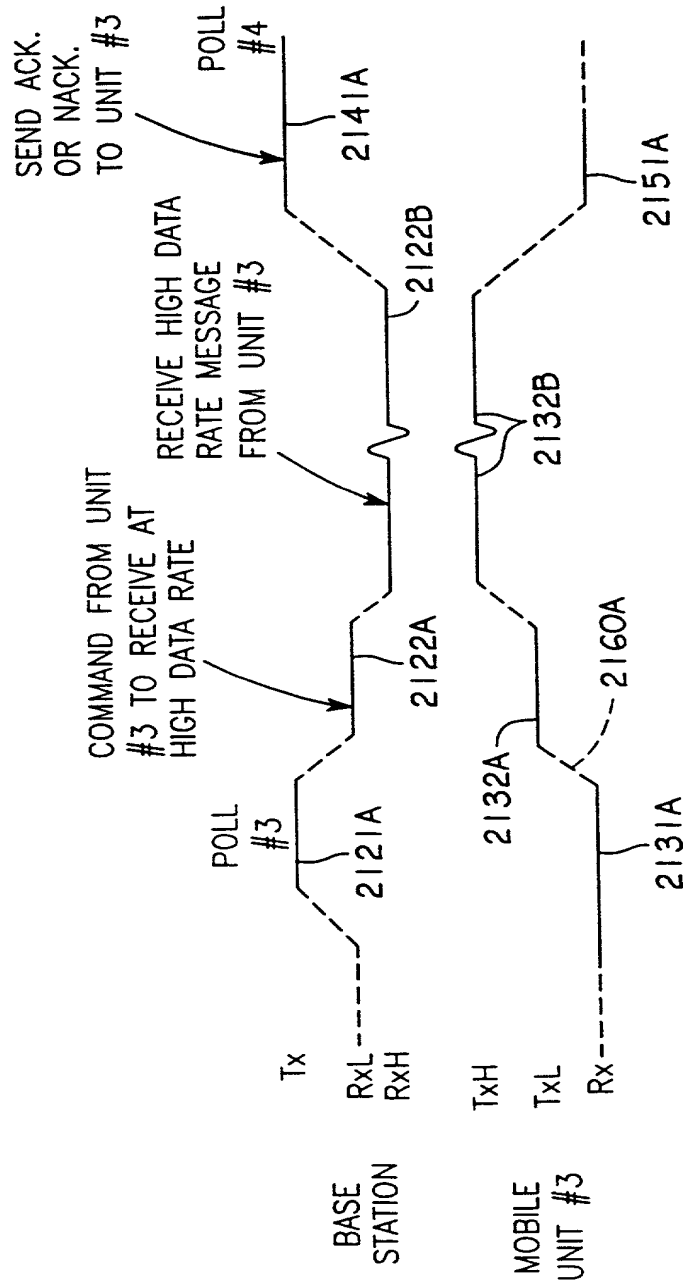


FIG. 25

FIG. 26

FIG. 29

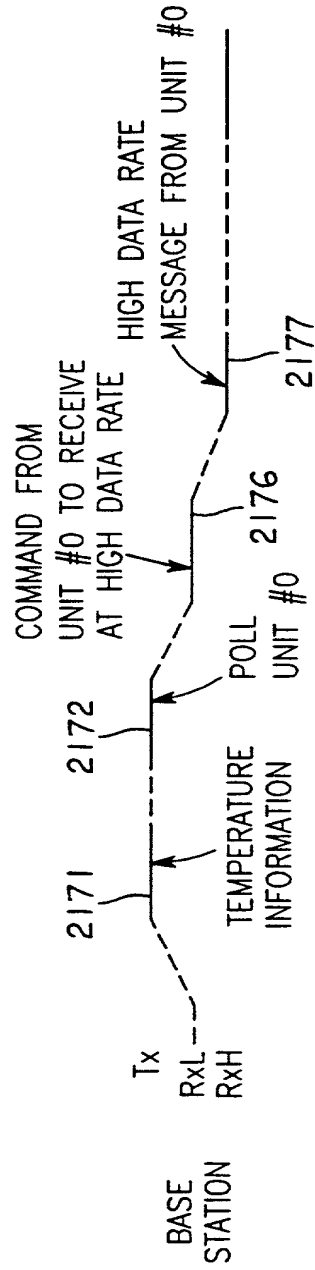
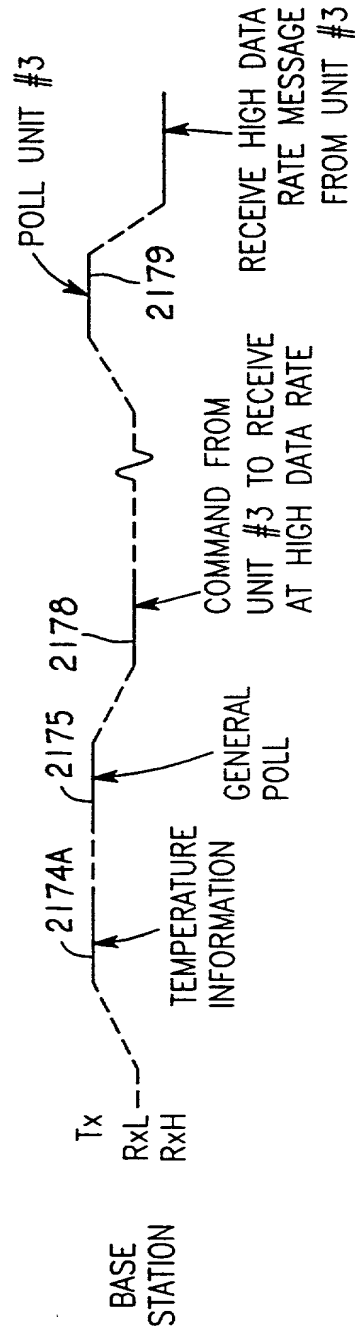


FIG. 30





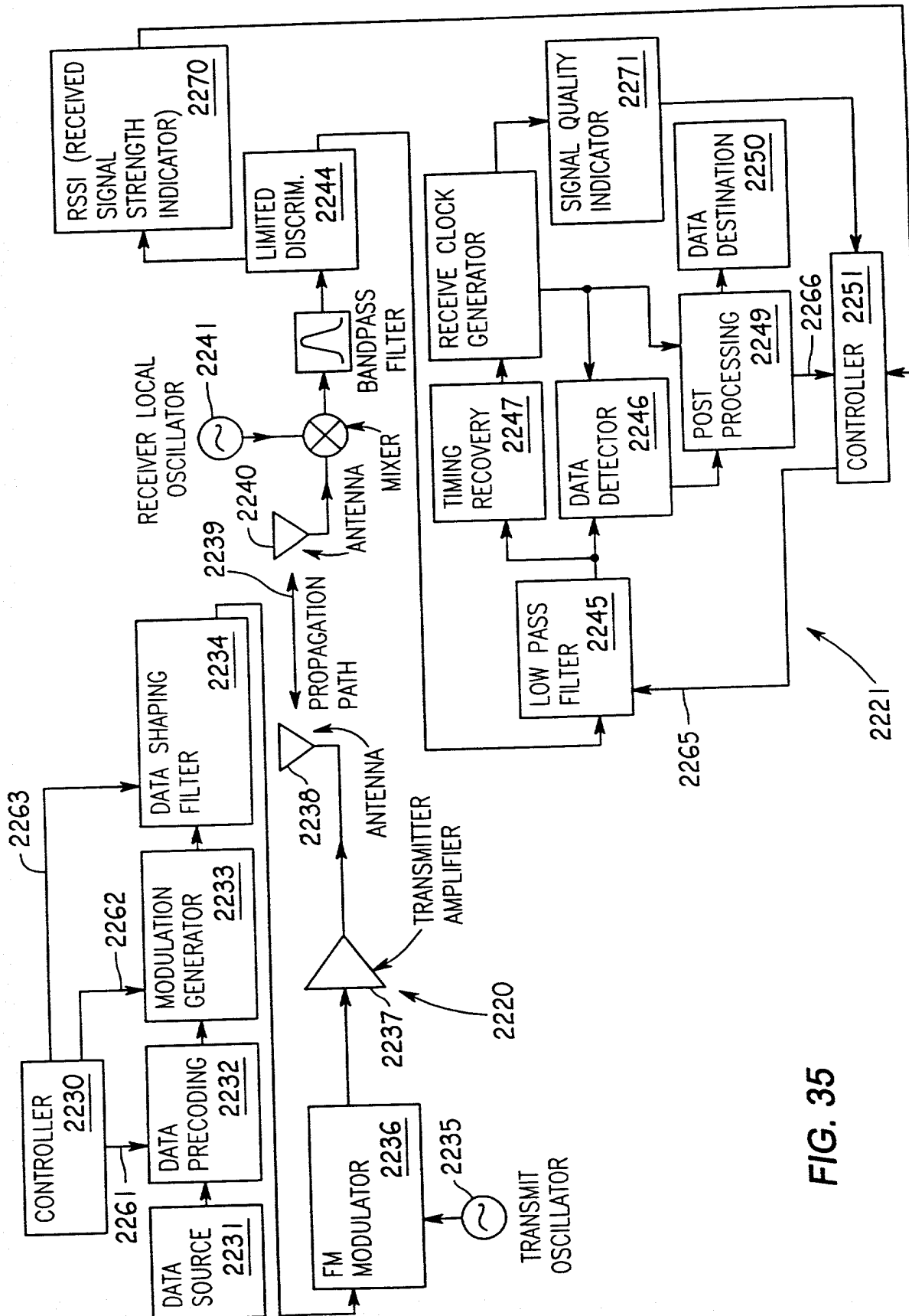
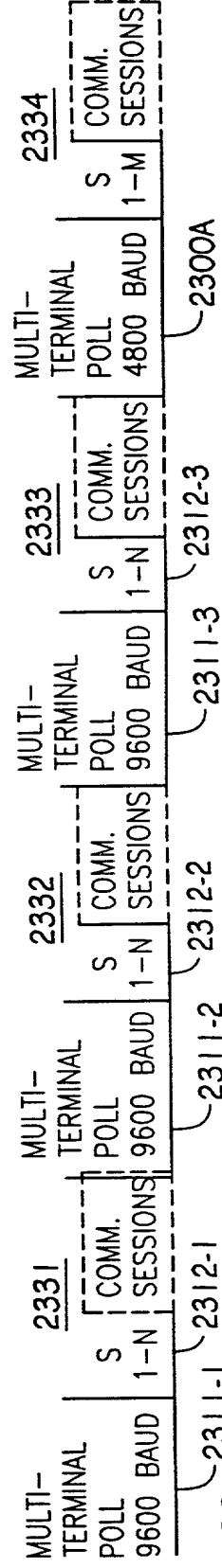
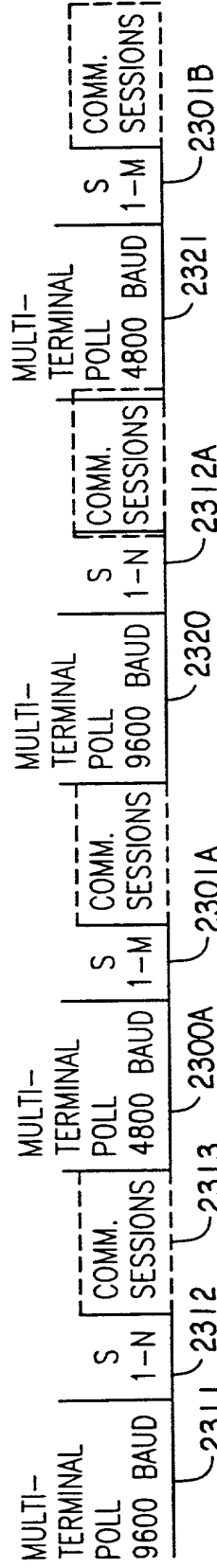
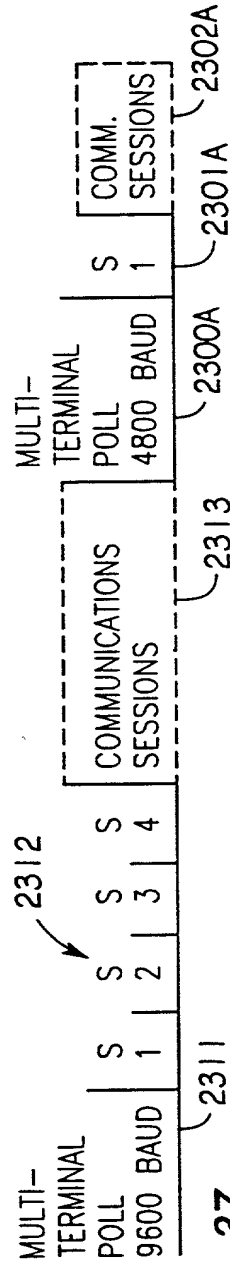
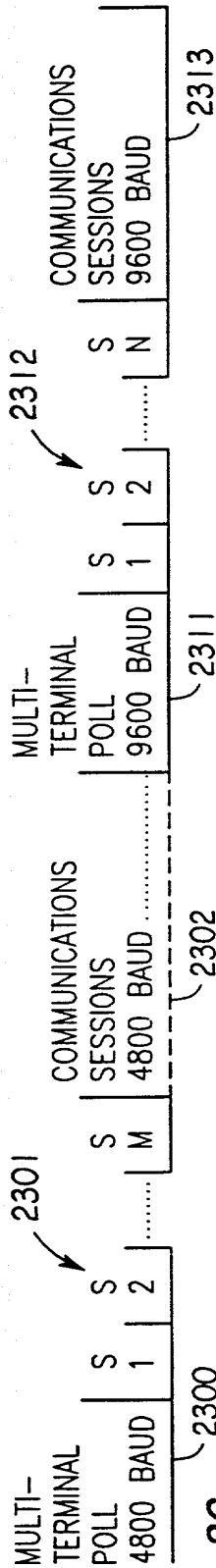


FIG. 35



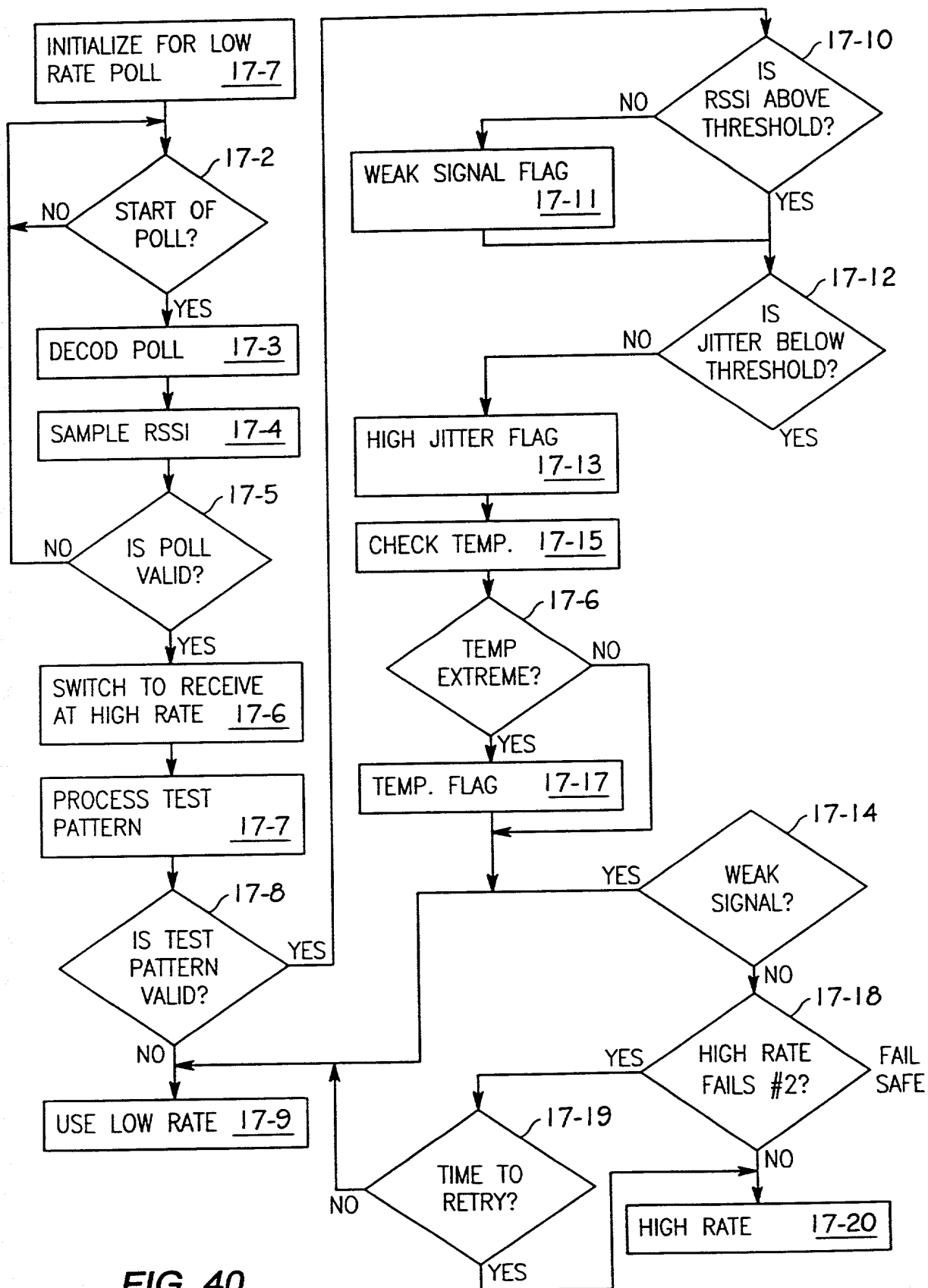
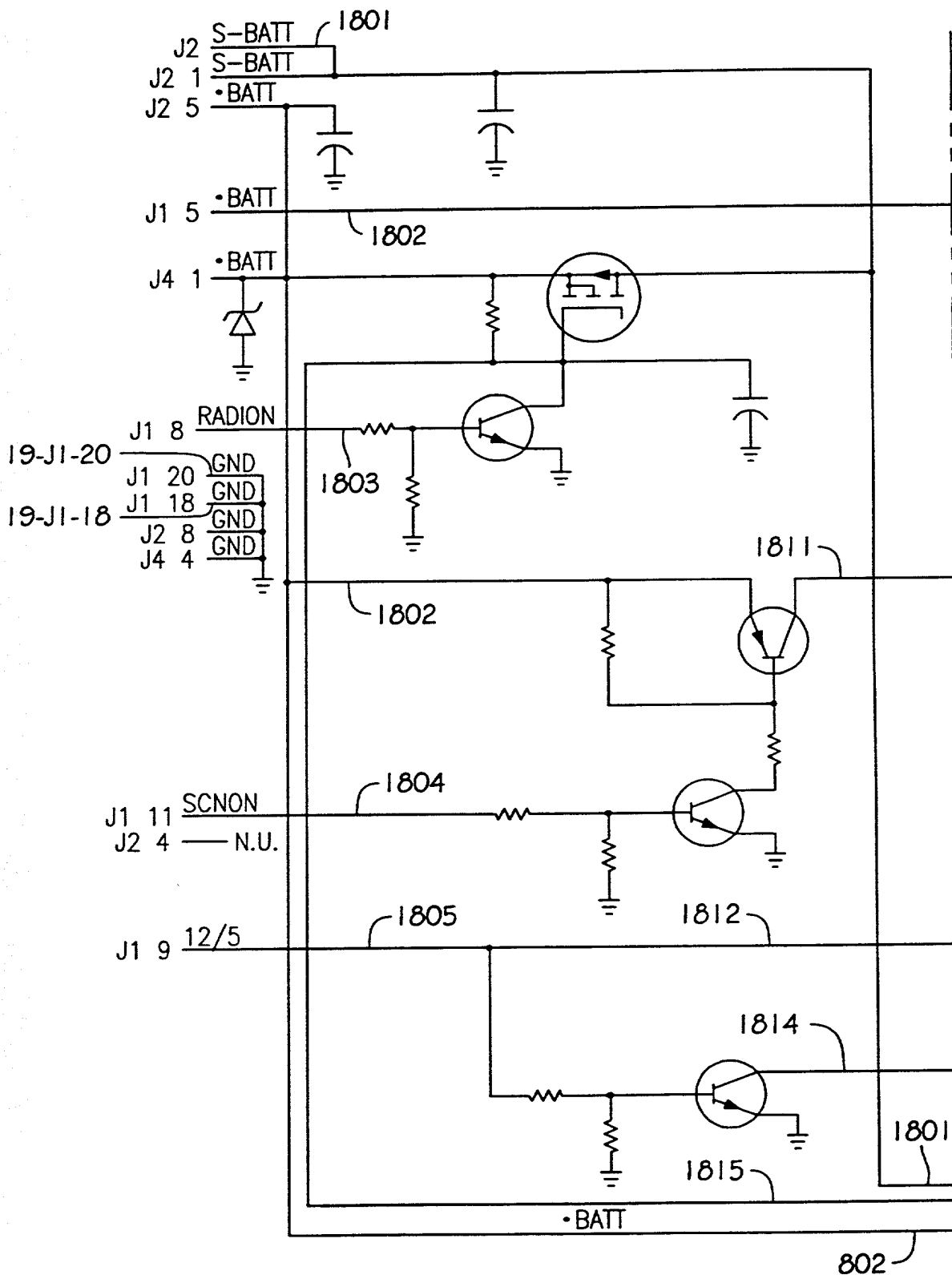


FIG. 40

28/69

FIG. 41A



29/69

FIG. 41B

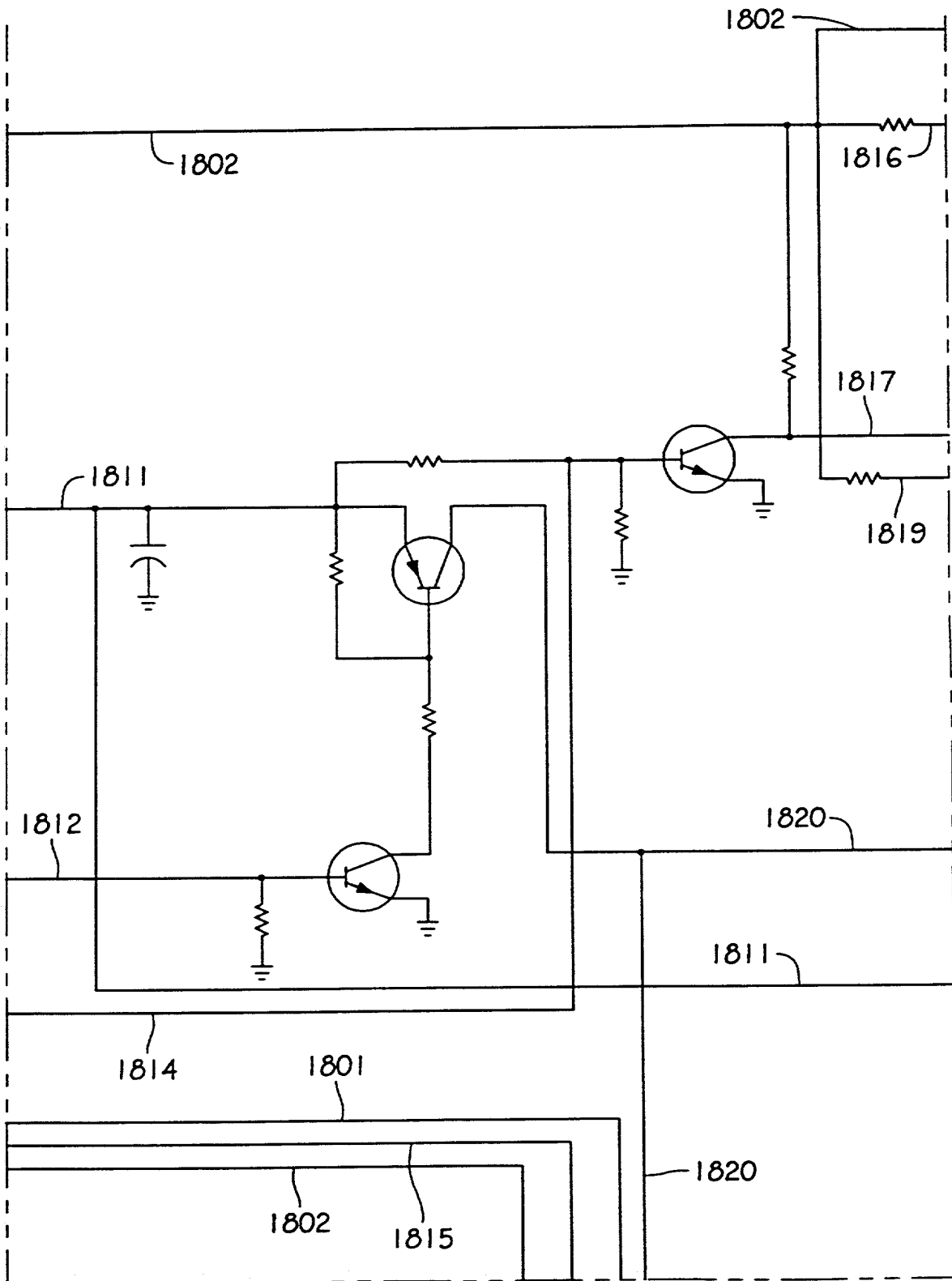
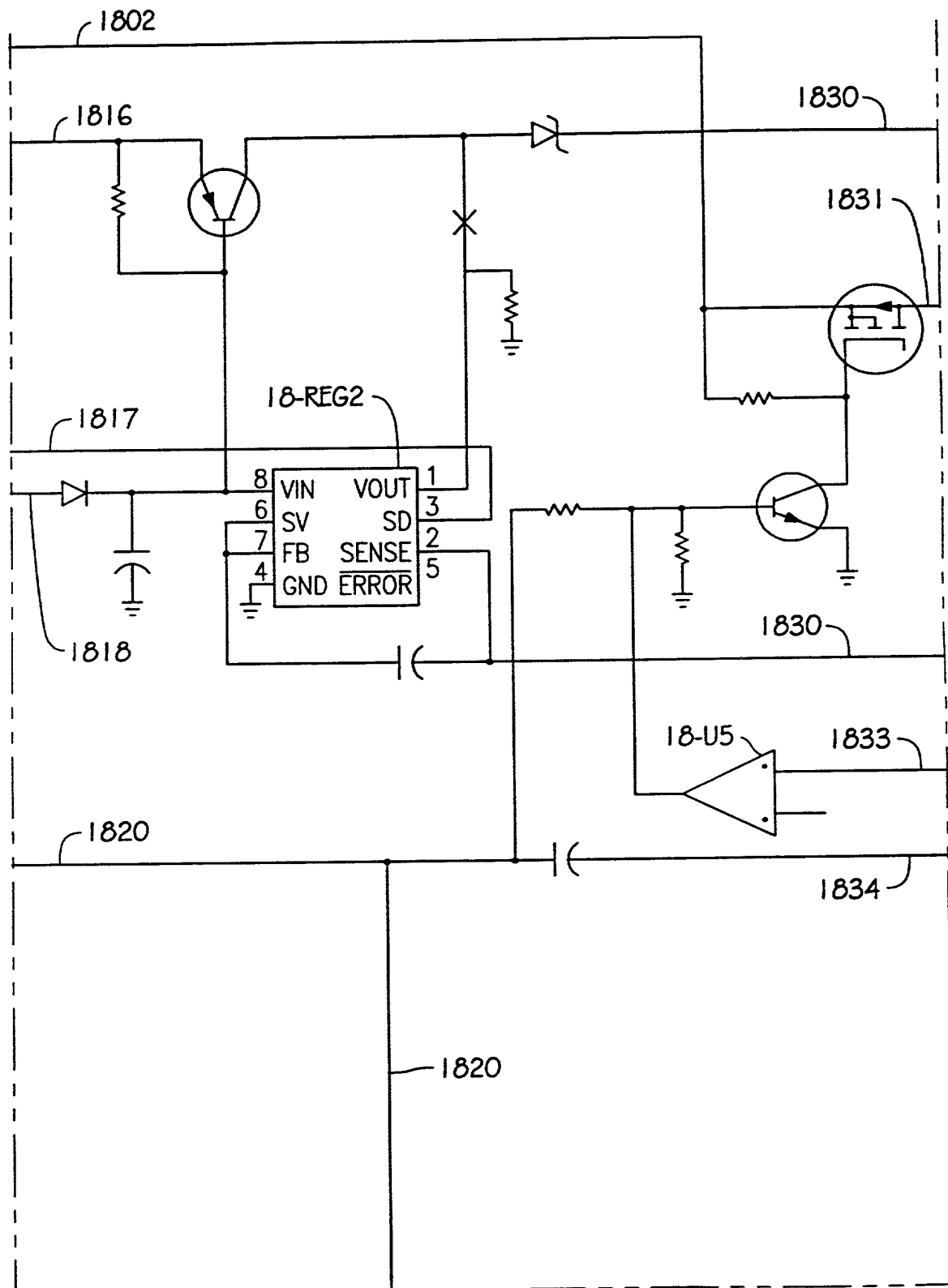


FIG. 41C



31/69

FIG. 41D

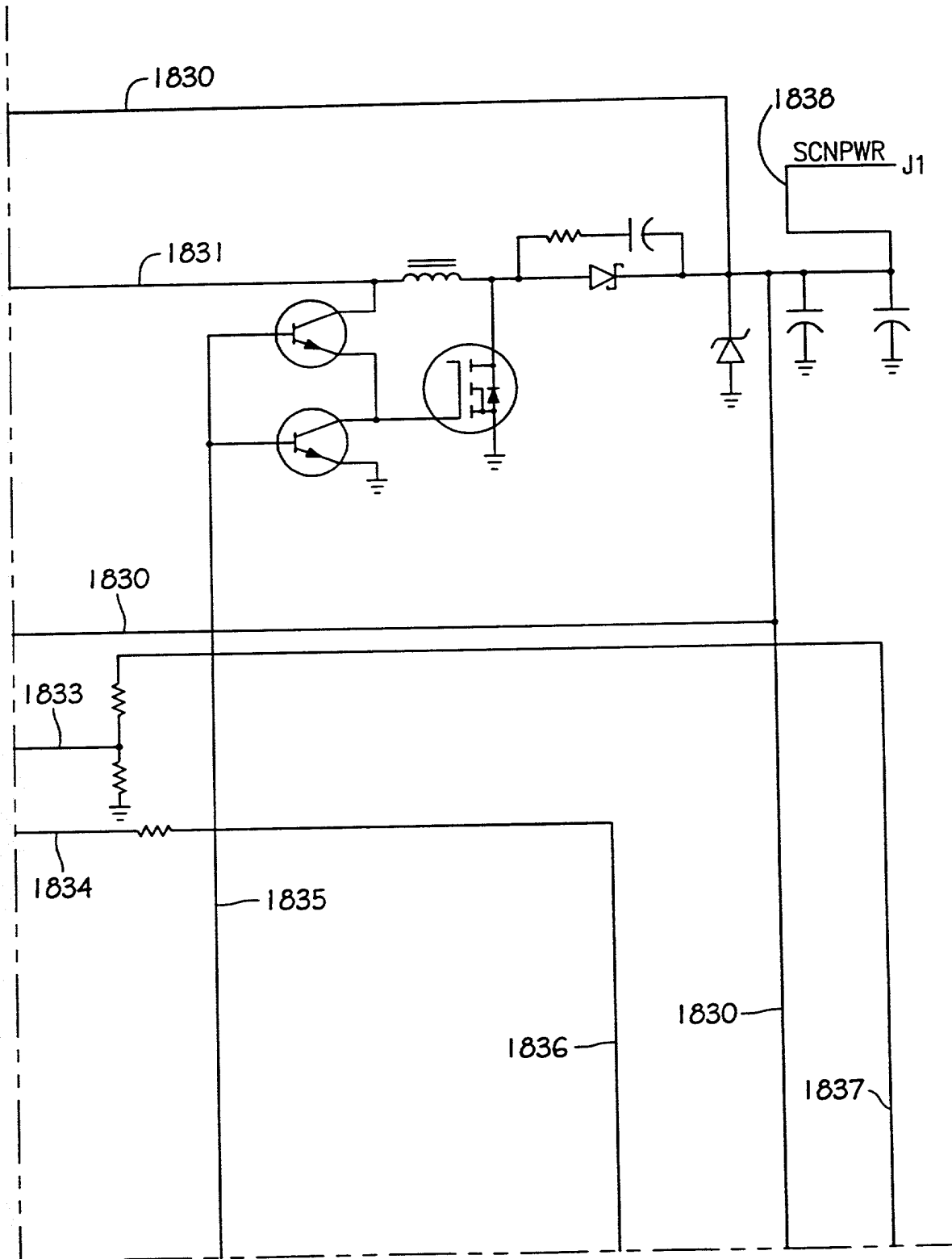


FIG. 41E

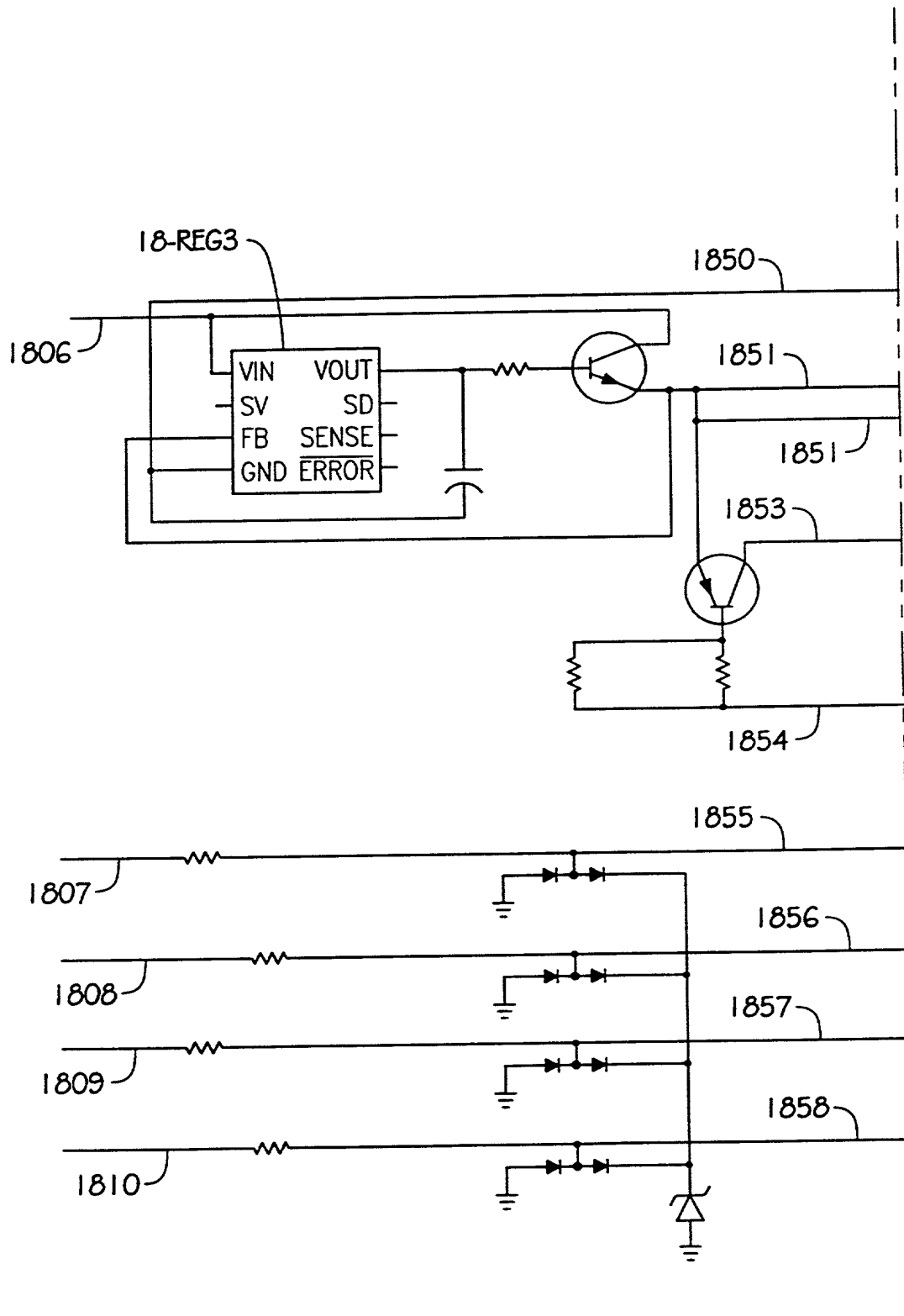




FIG. 41F

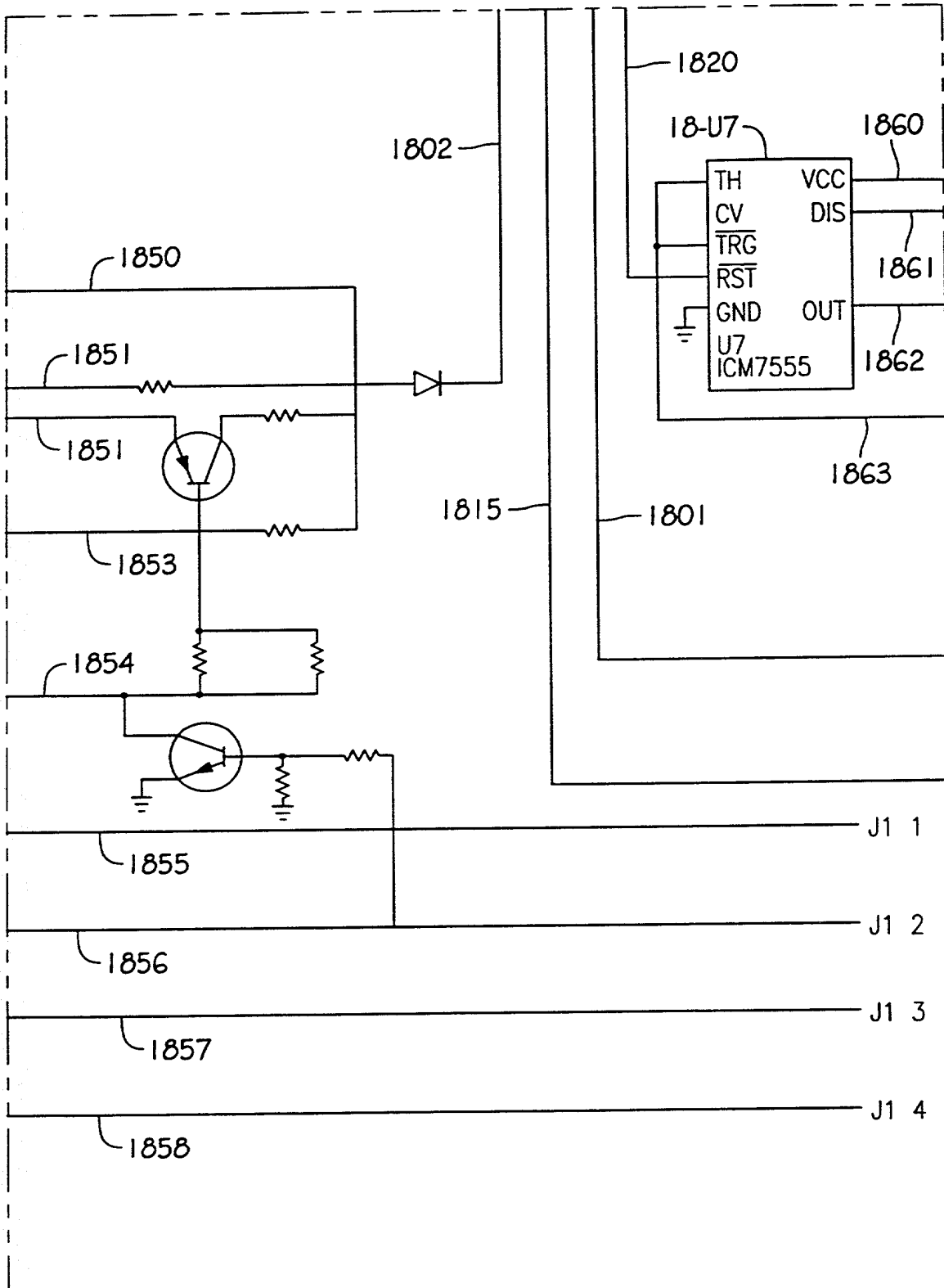


FIG. 41G

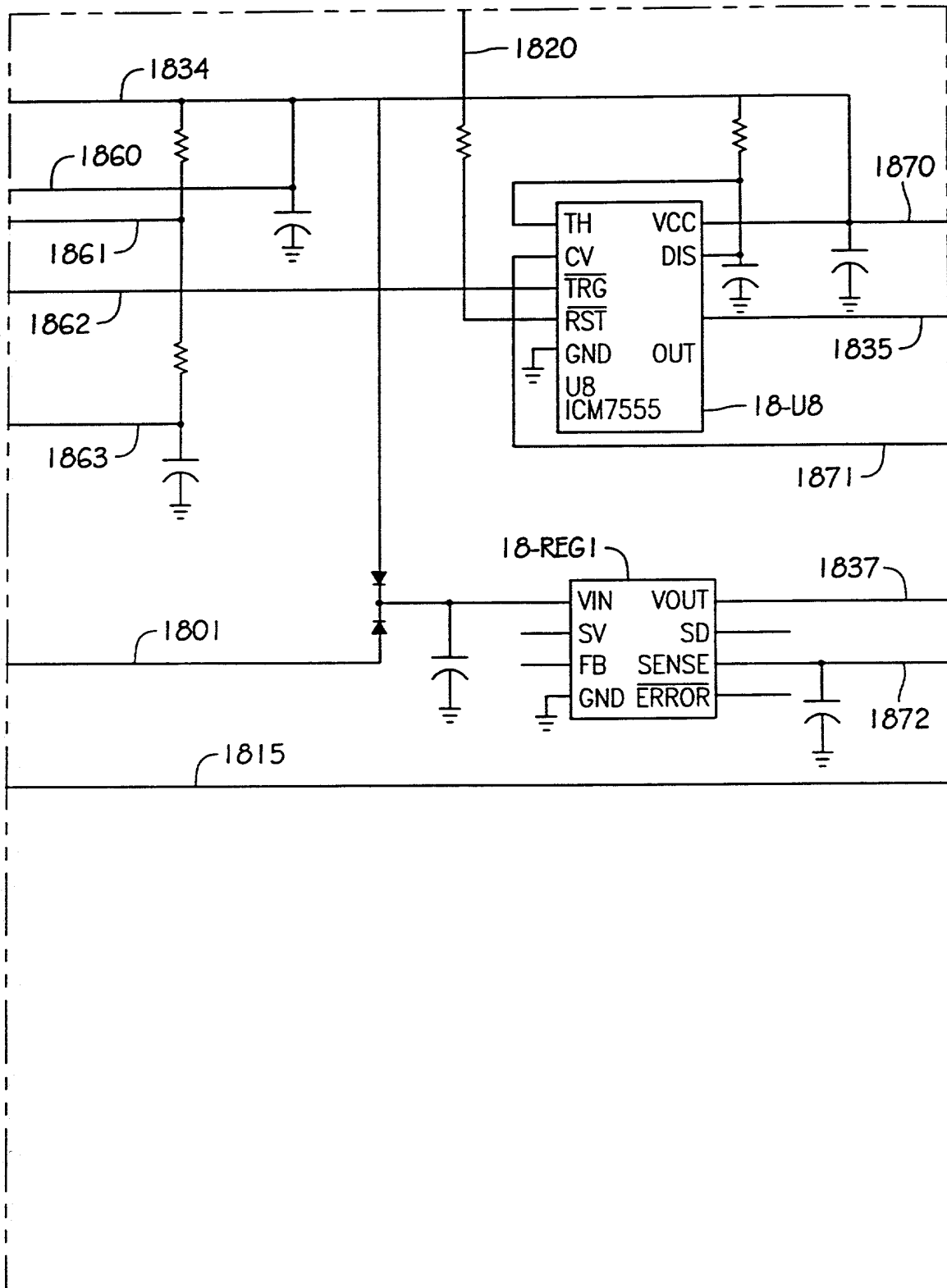


FIG. 41H

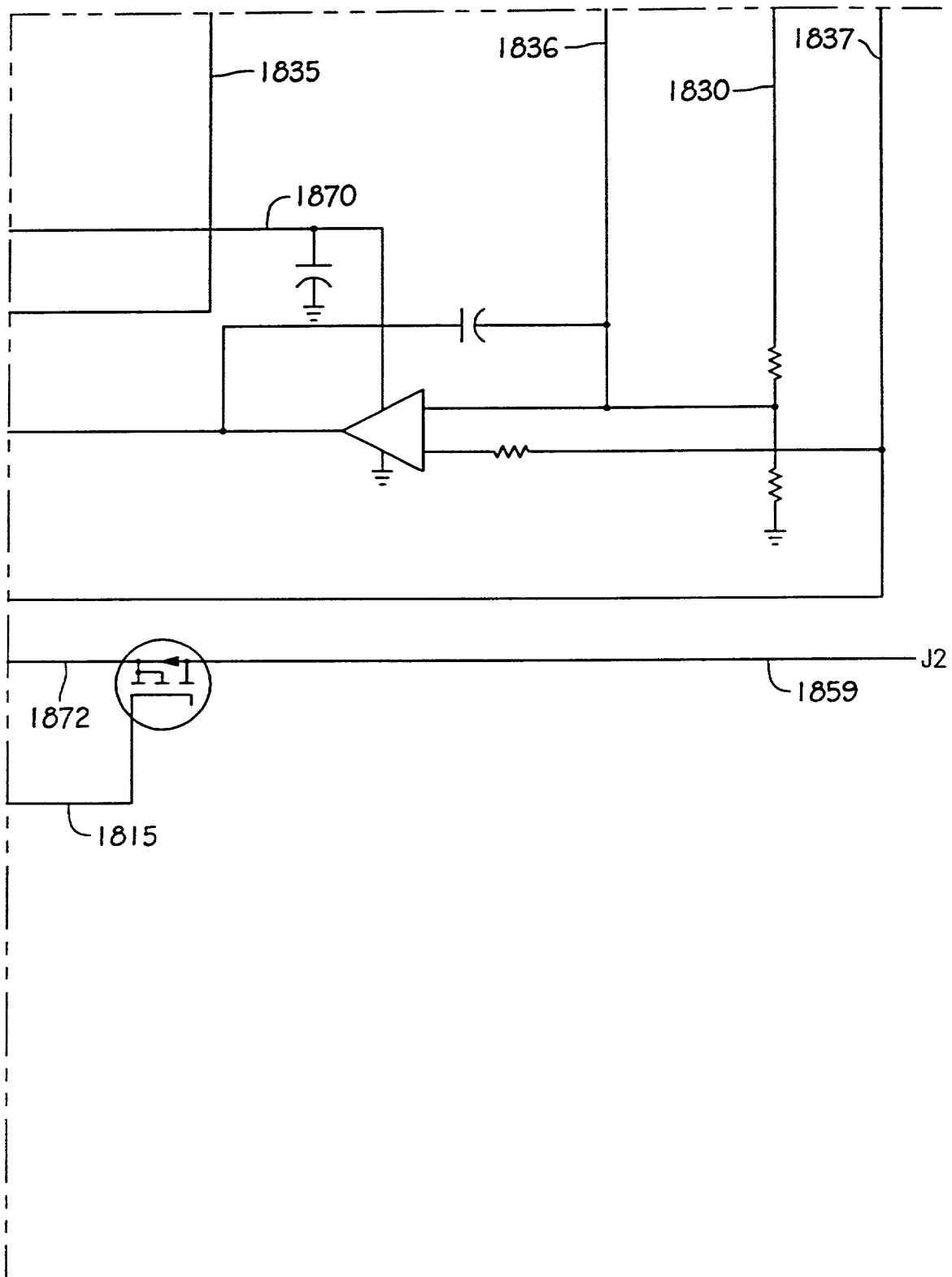
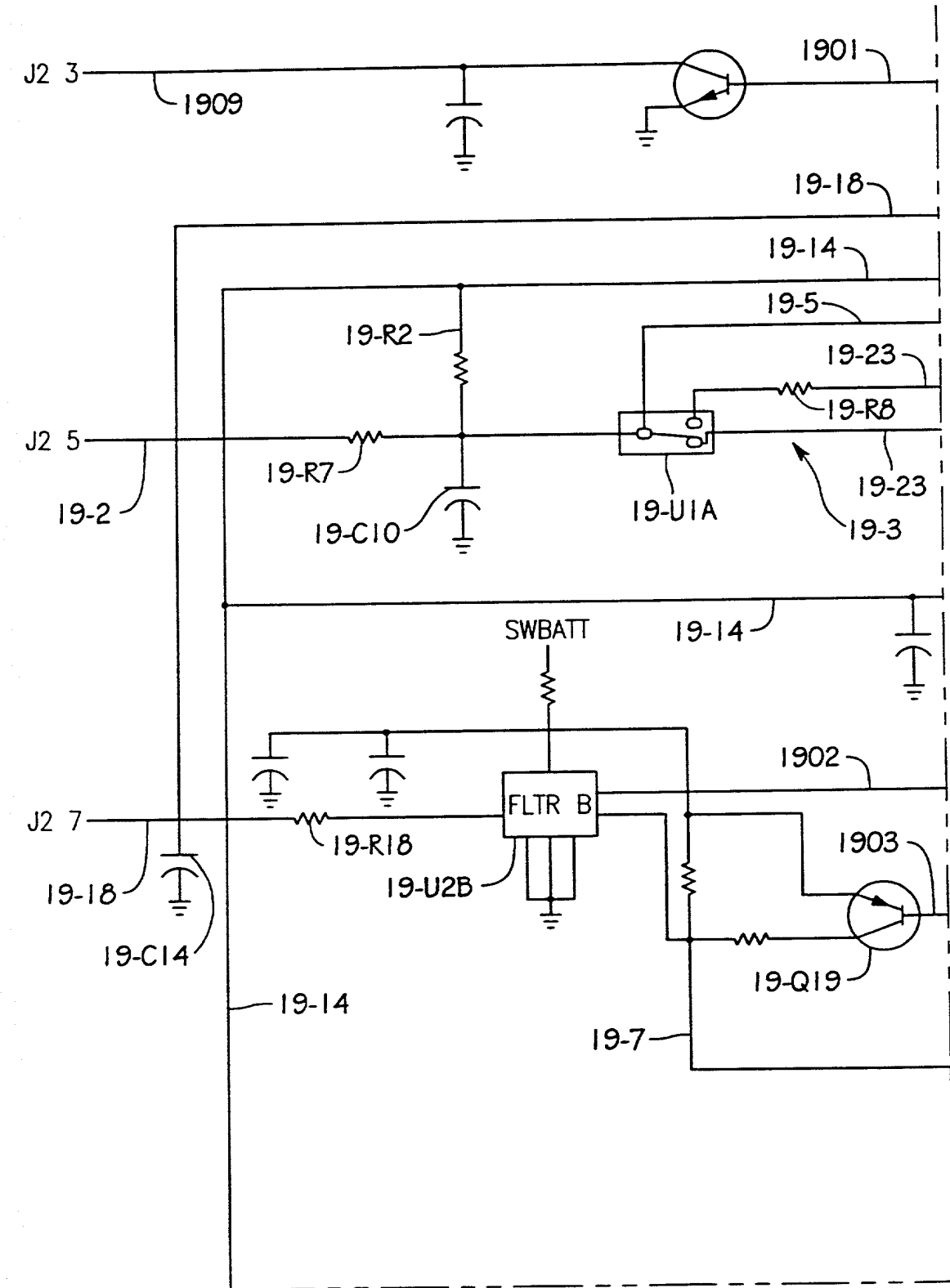


FIG. 42A



**FIG. 42B**

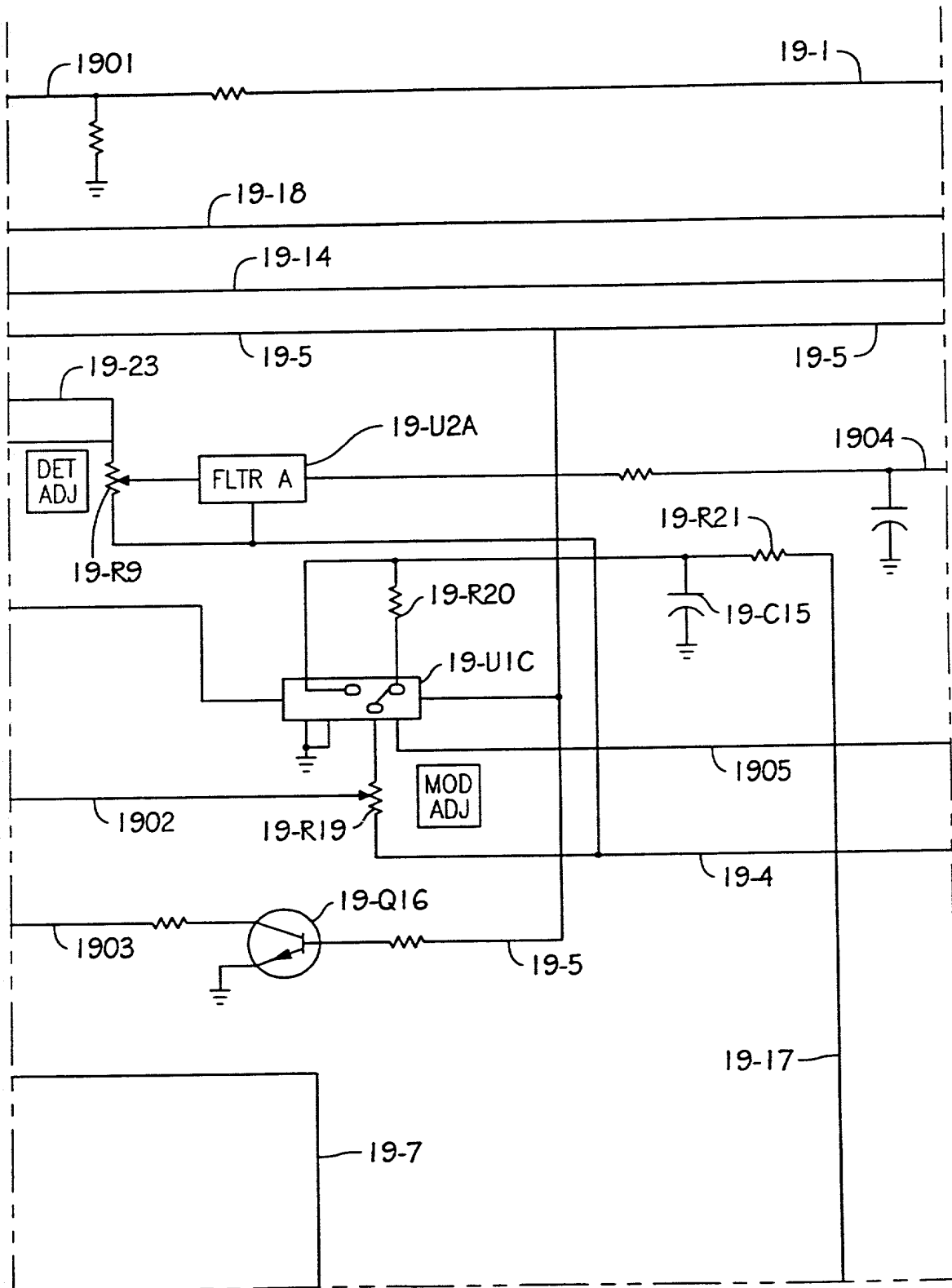


FIG. 42C

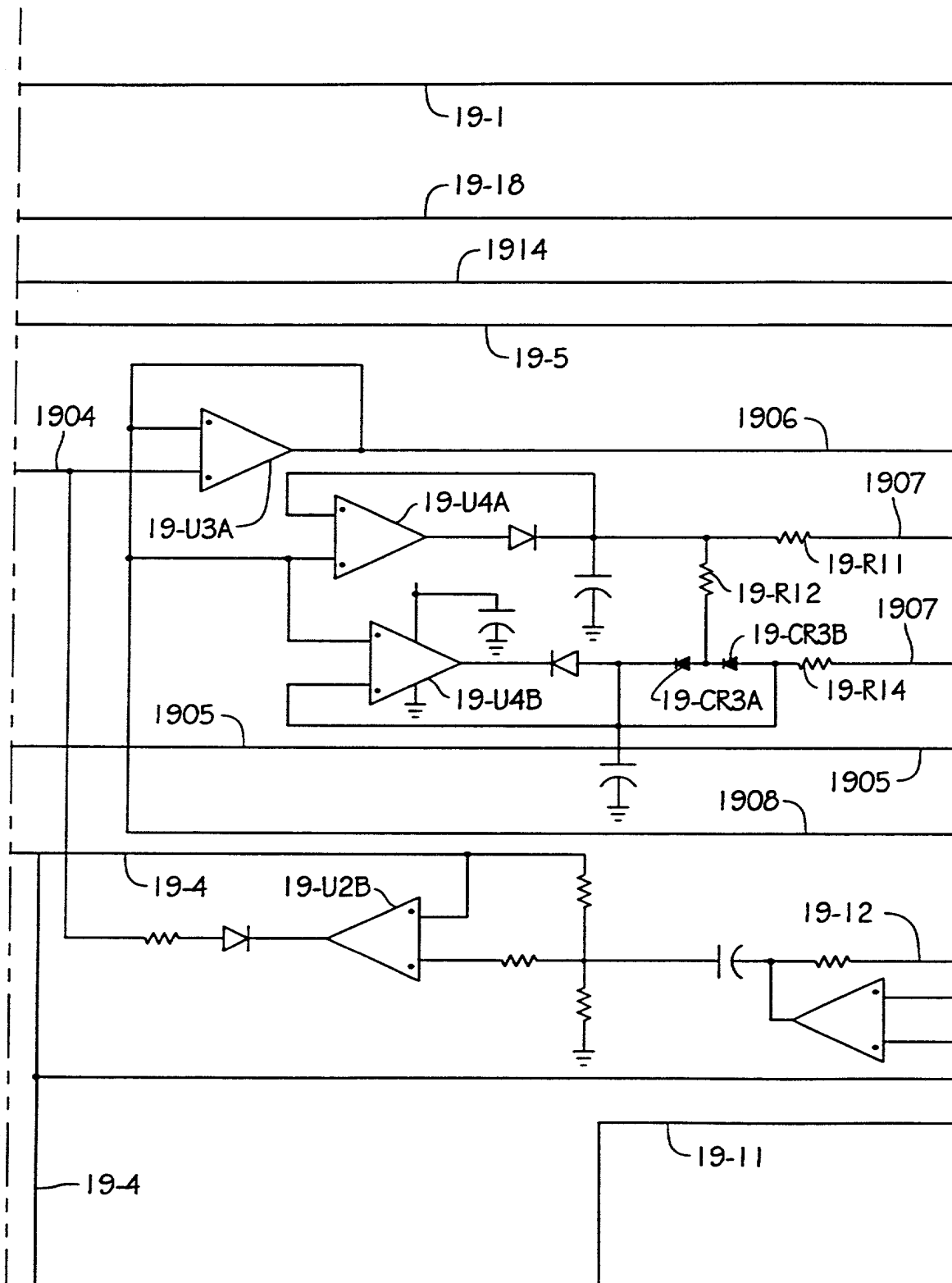


FIG. 42D

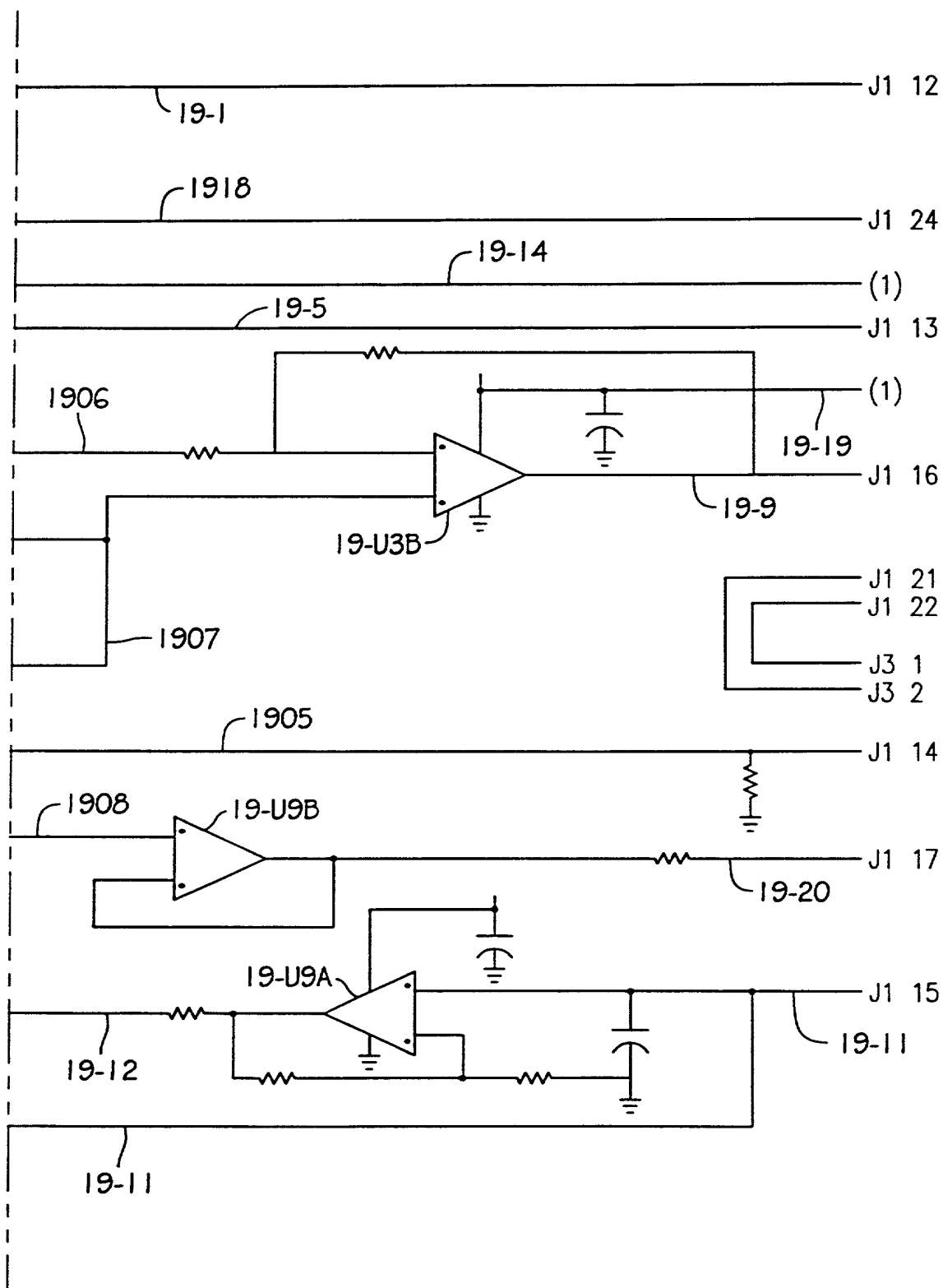
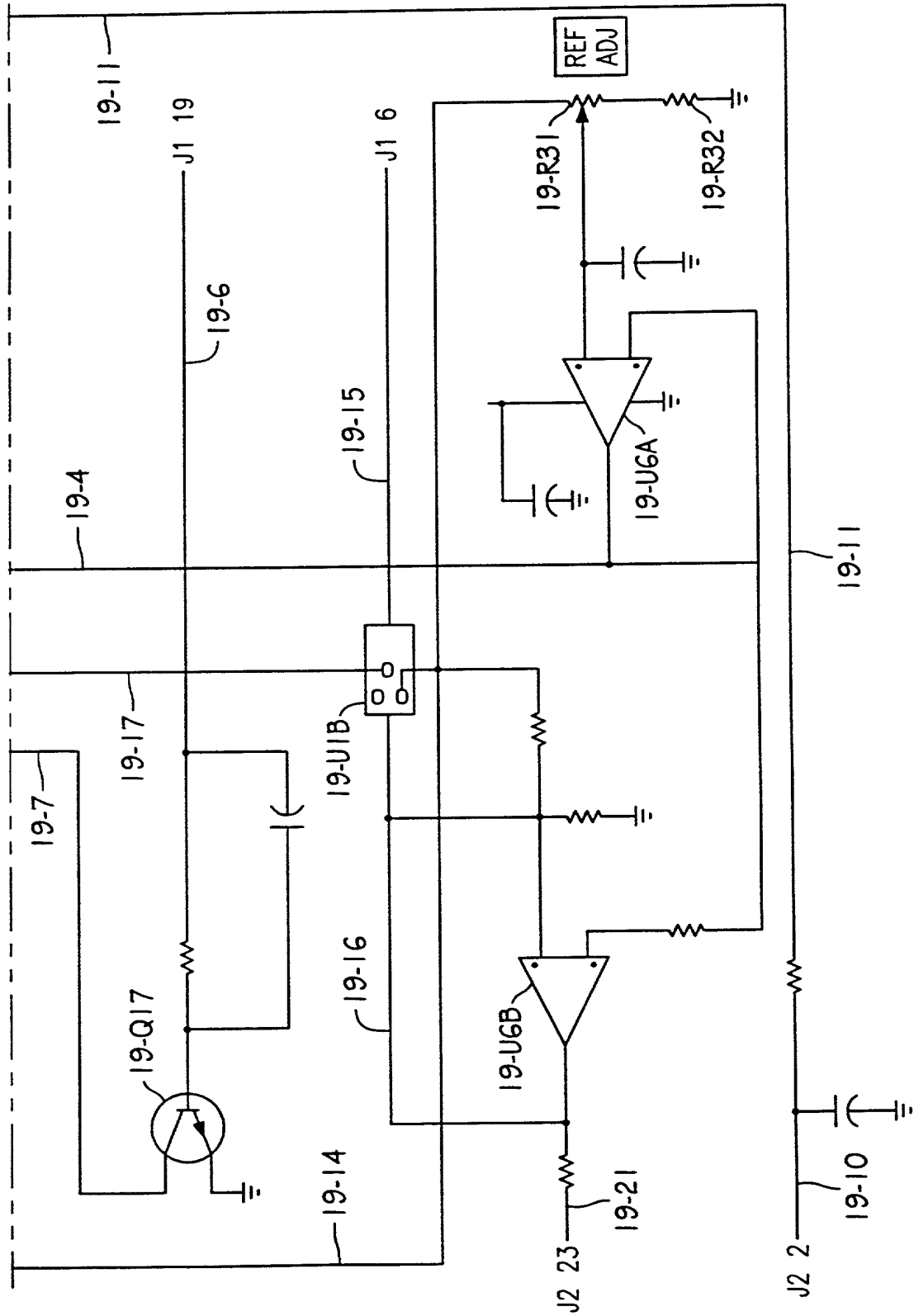


FIG. 42E





41/69

FIG. 43A

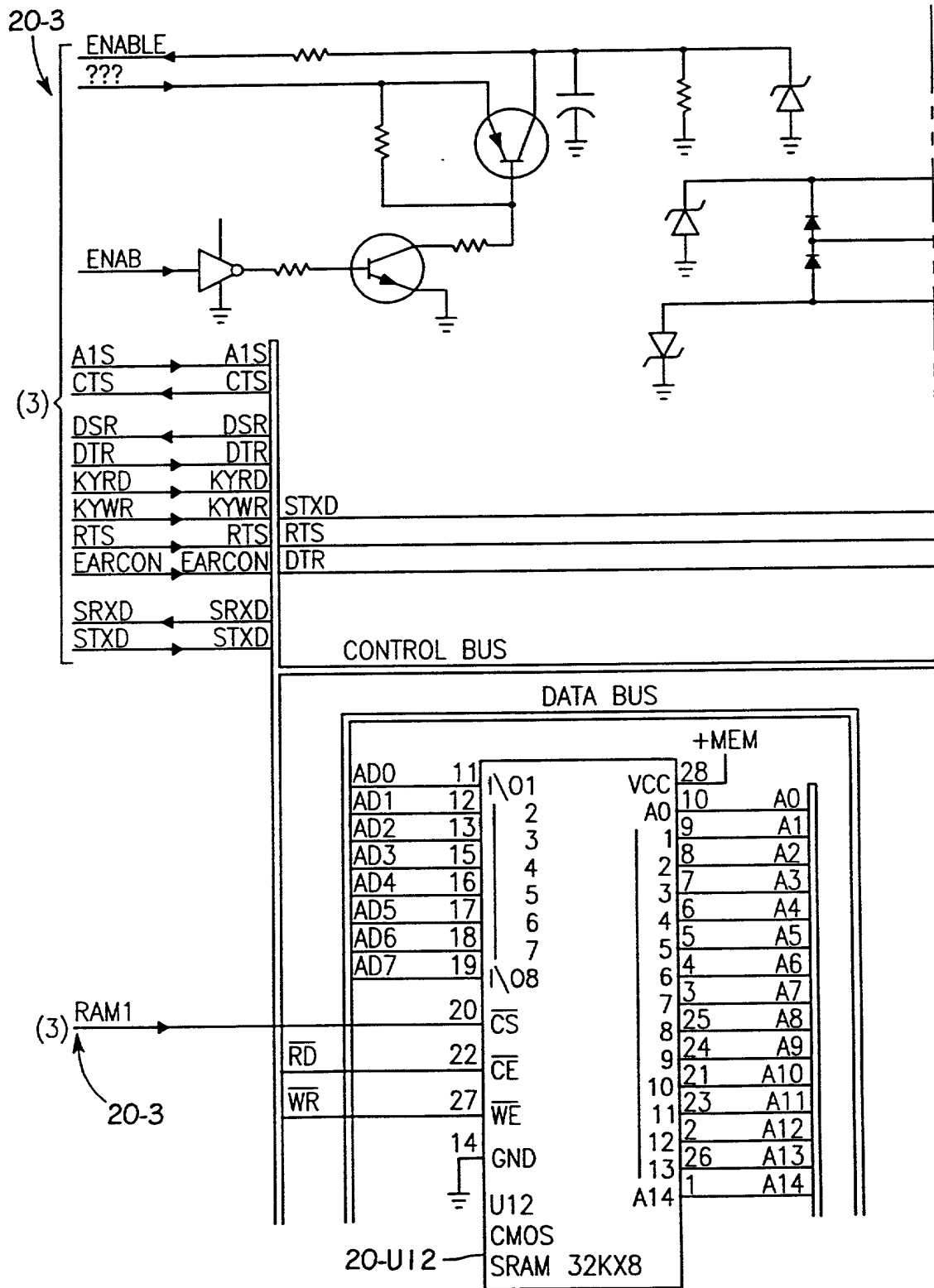


FIG. 43B

42/69

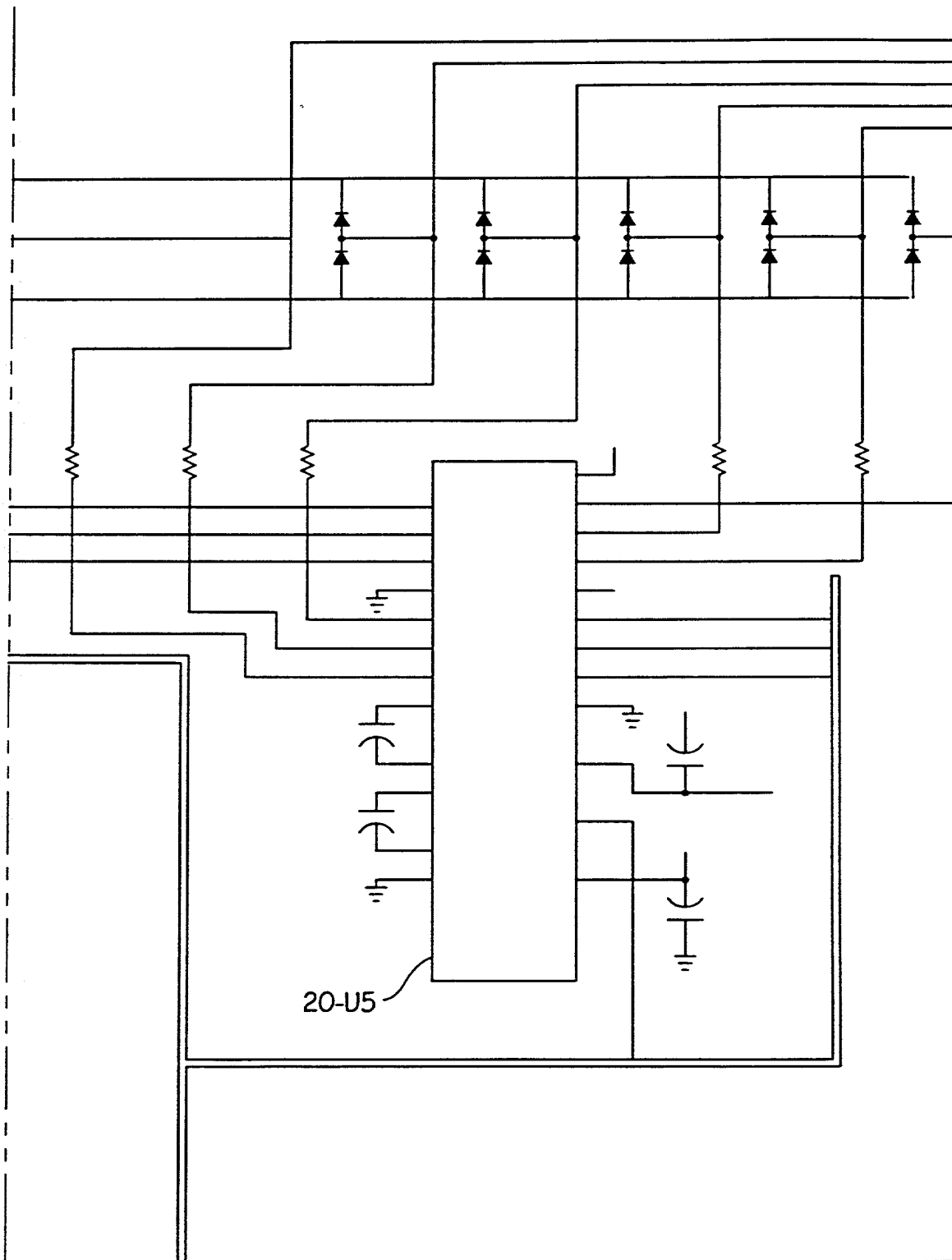


FIG. 43C

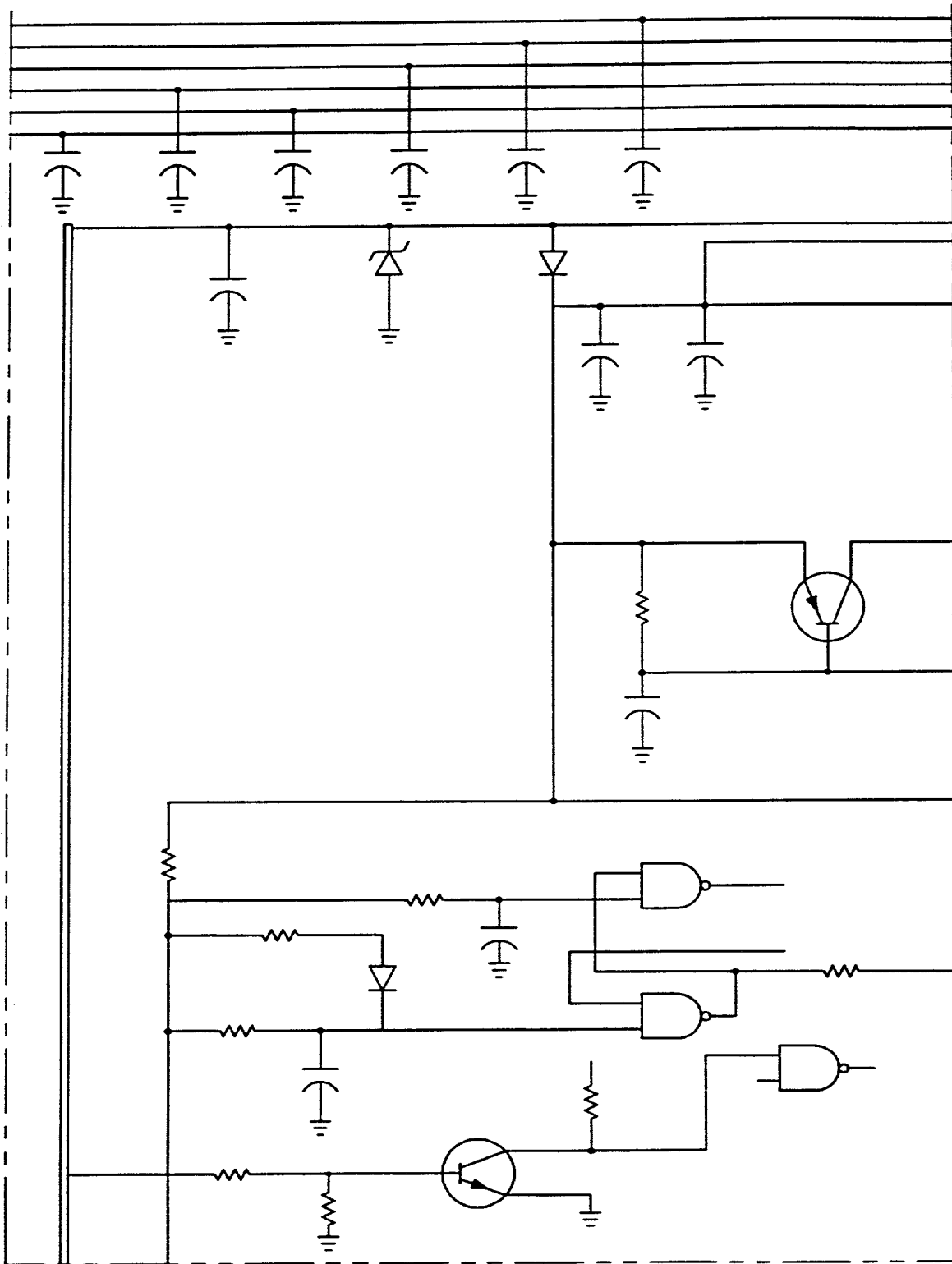


FIG. 43D

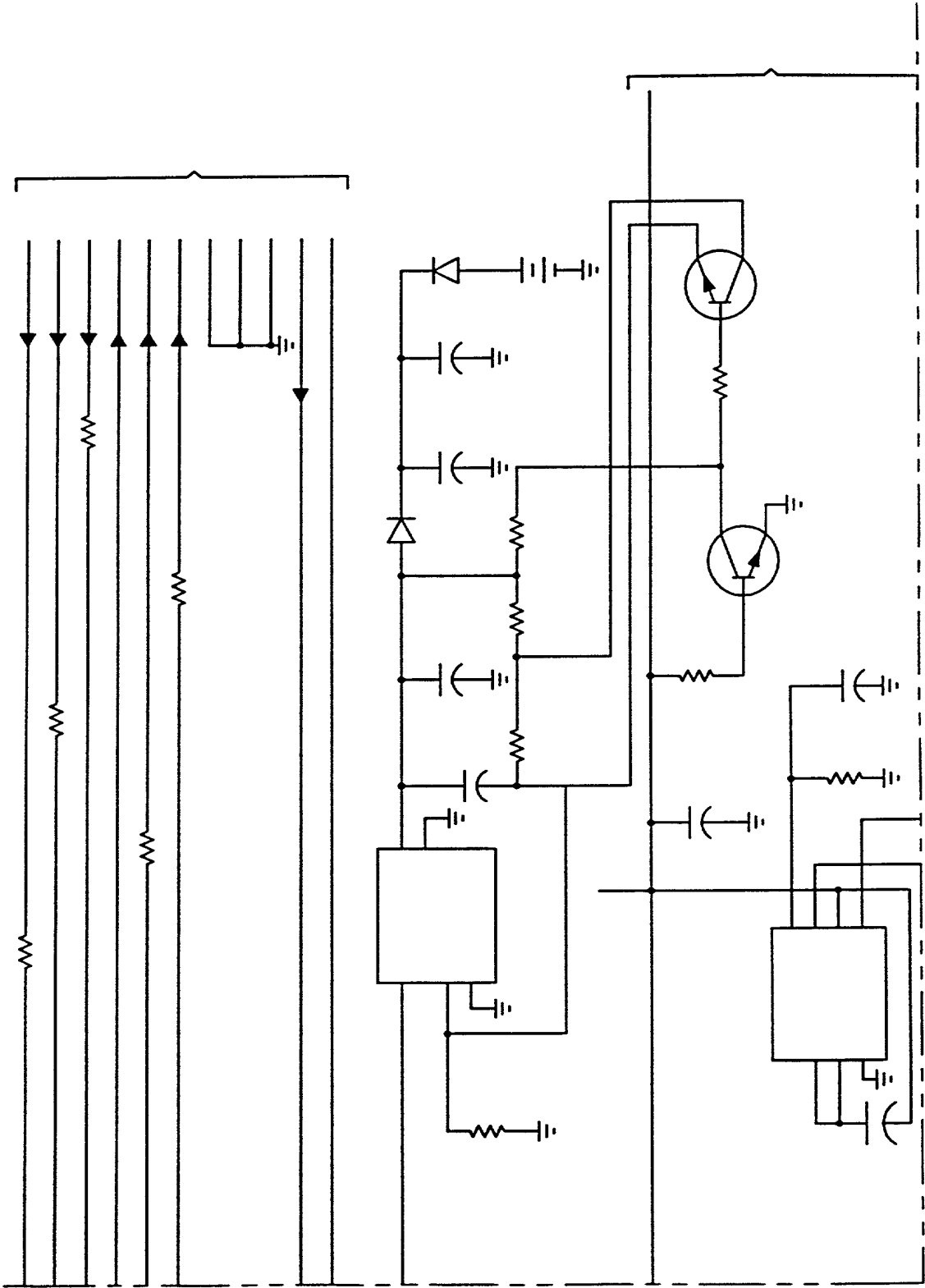


FIG. 43E

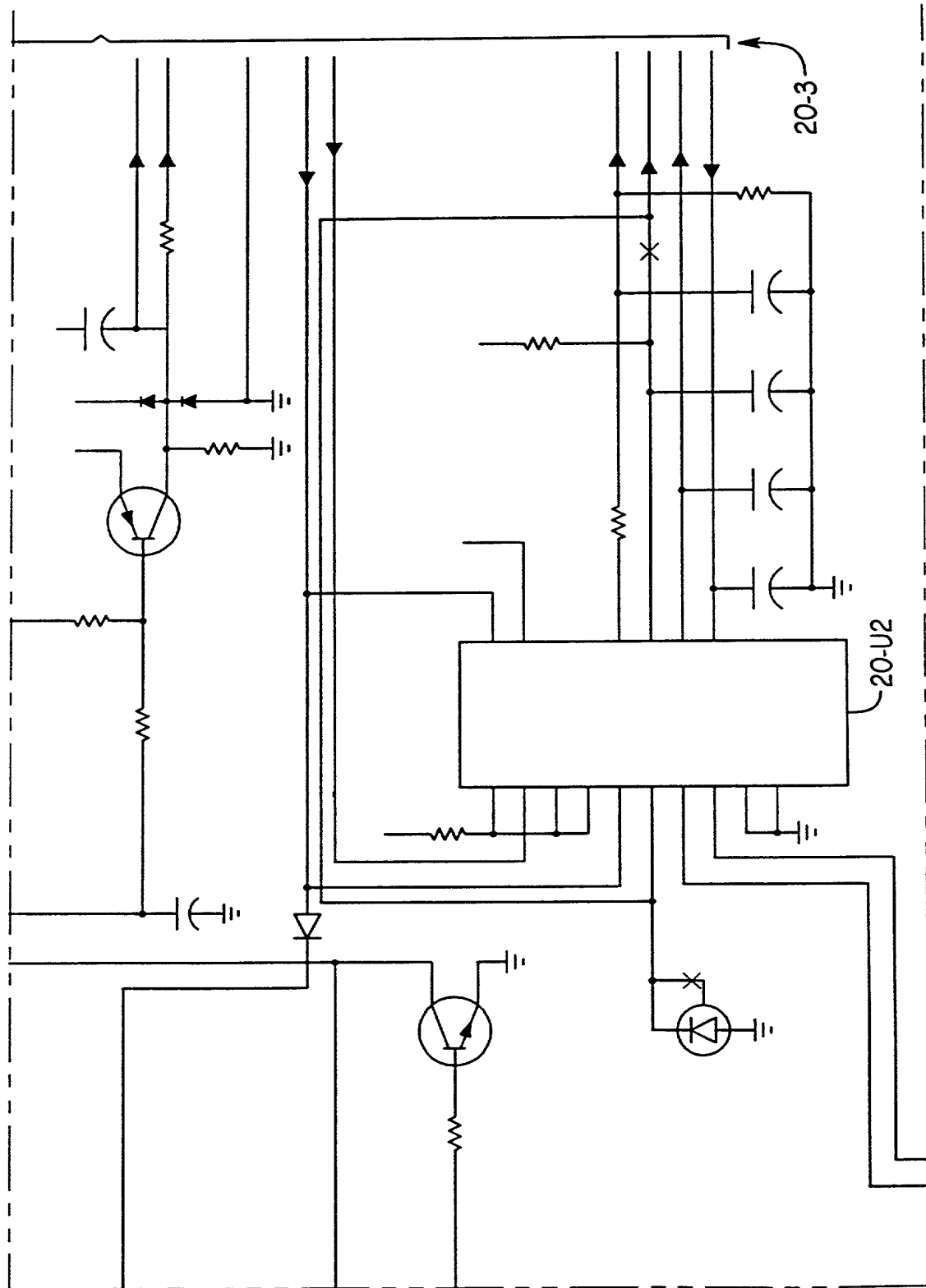


FIG. 43F

46/69

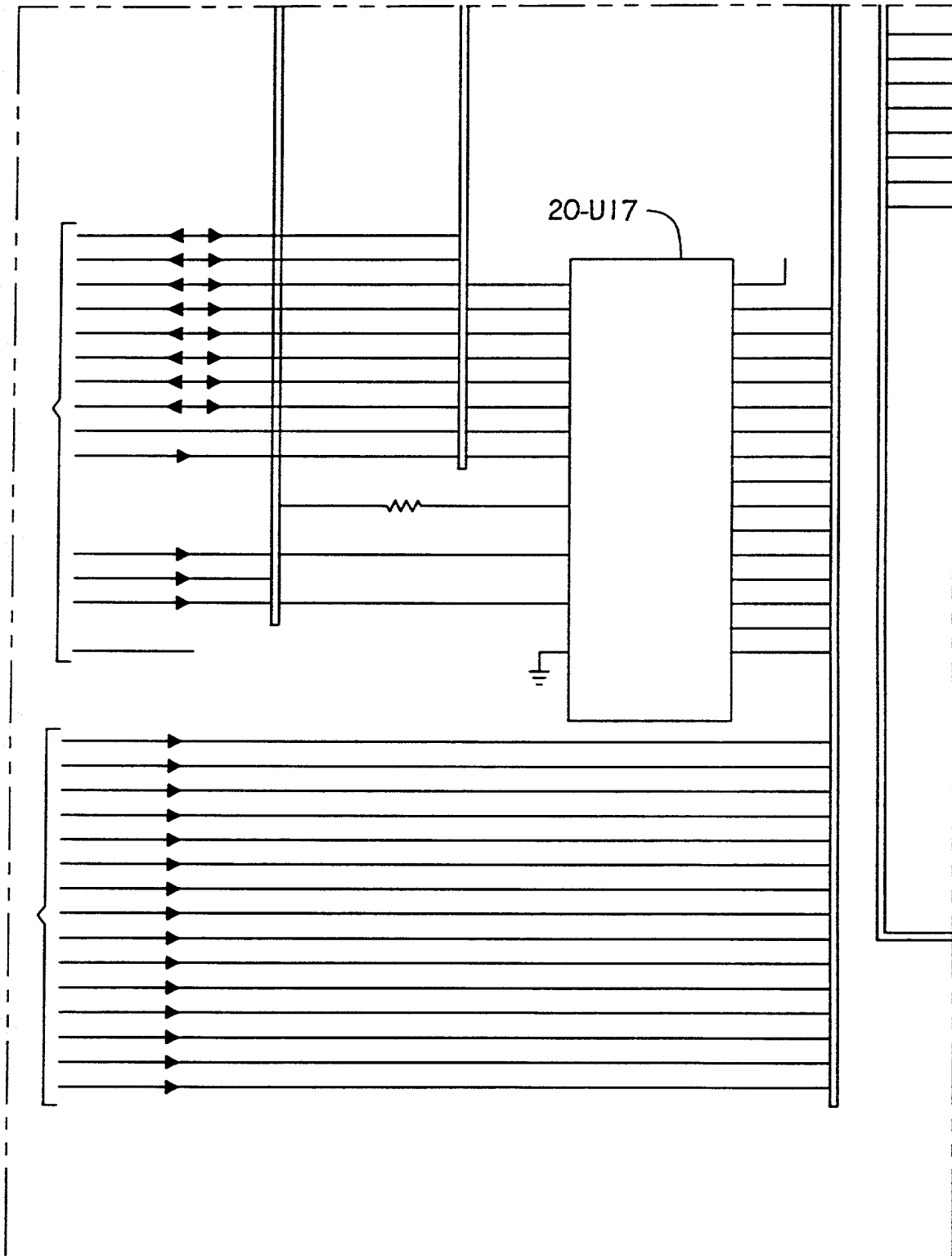


FIG. 43G

47/69

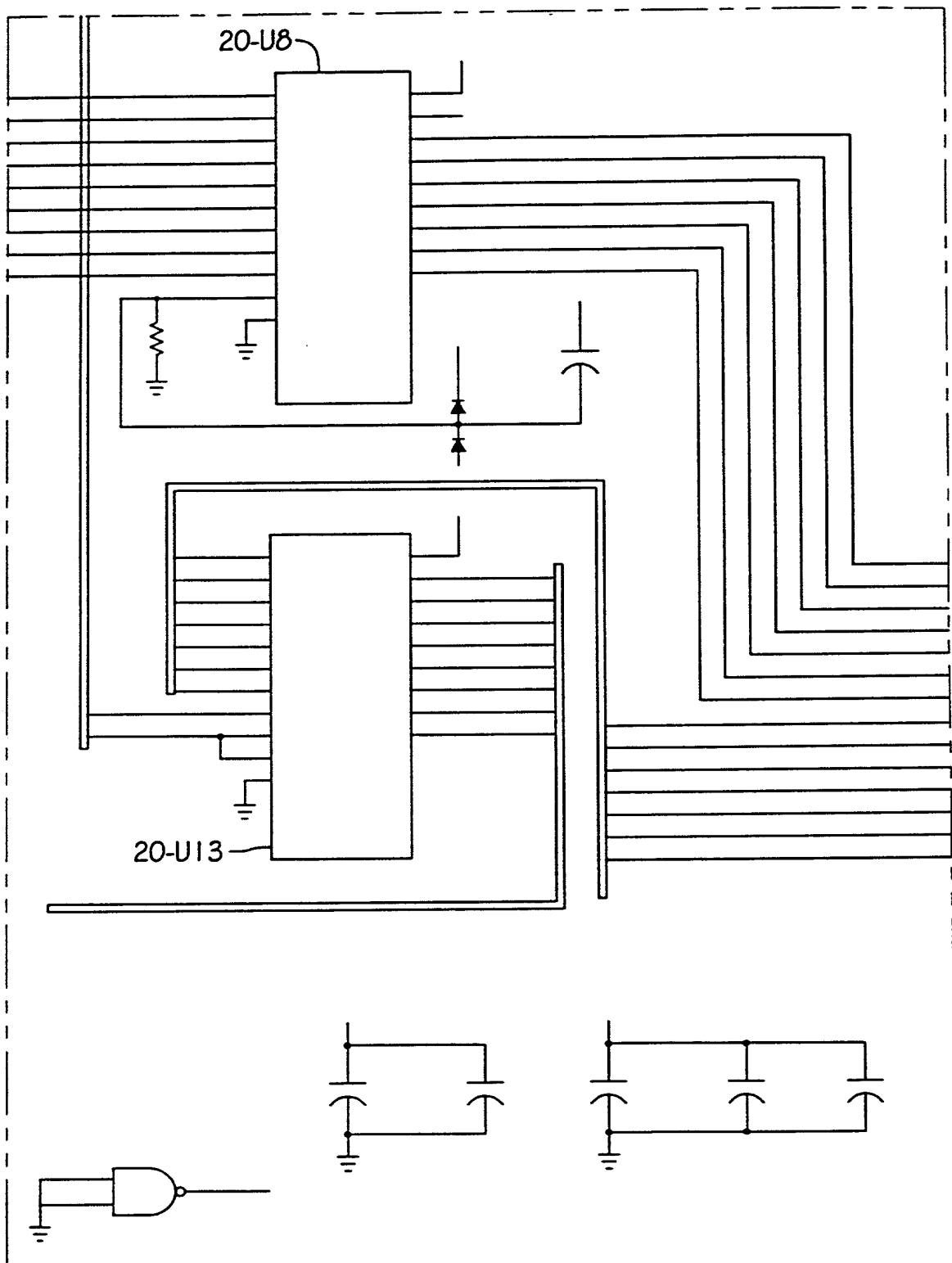


FIG. 43H

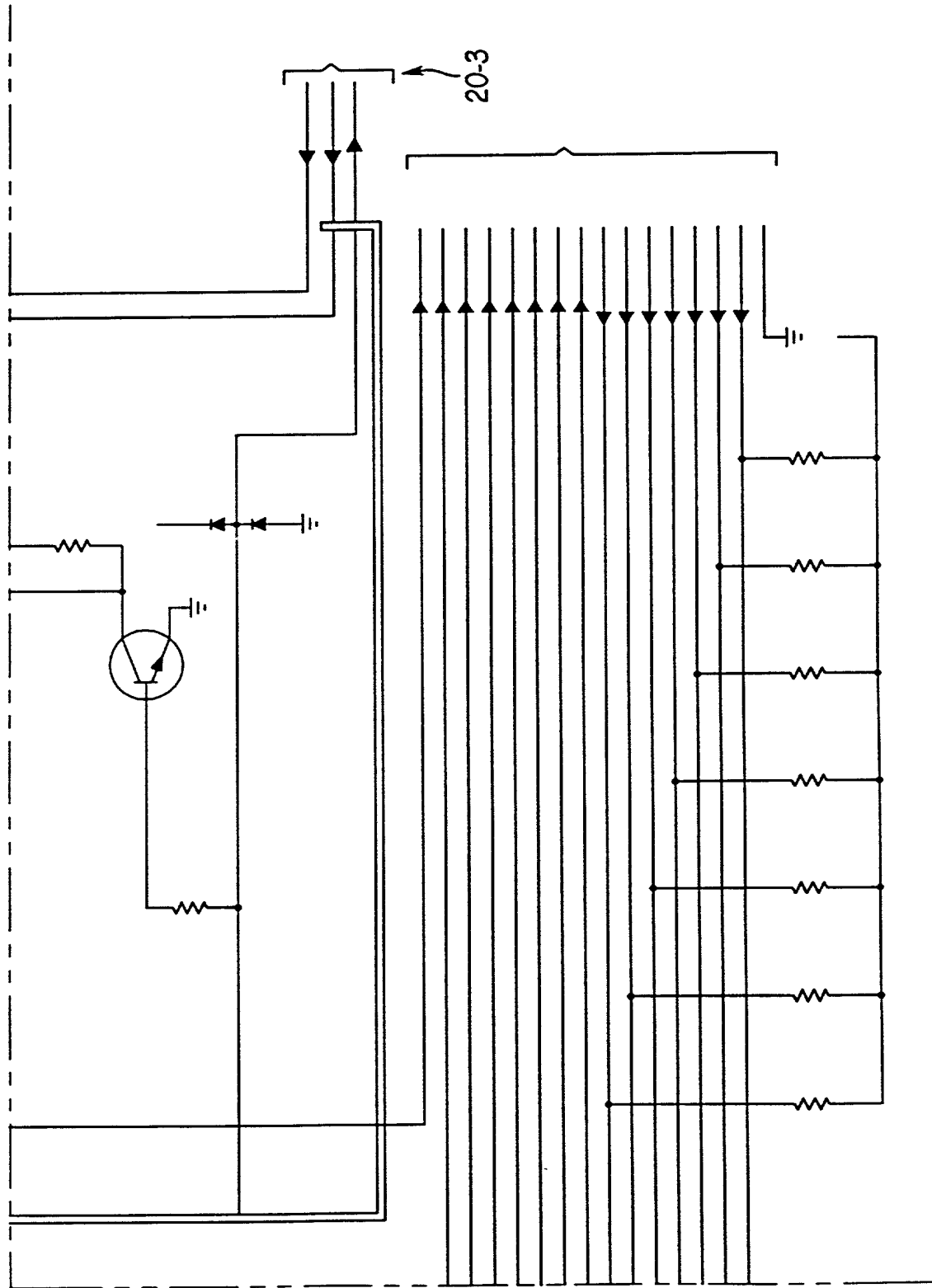




FIG. 44A

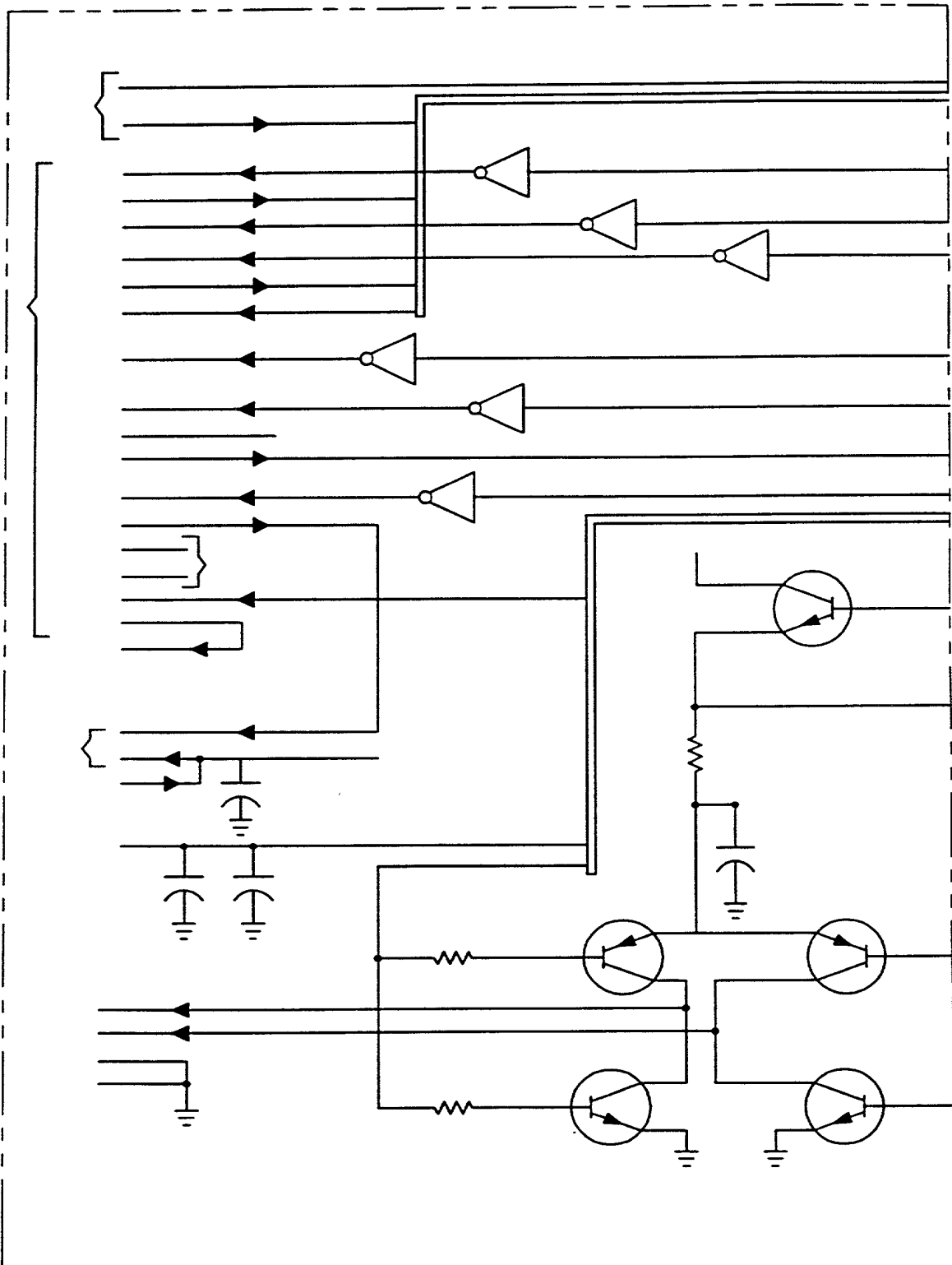


FIG. 44B

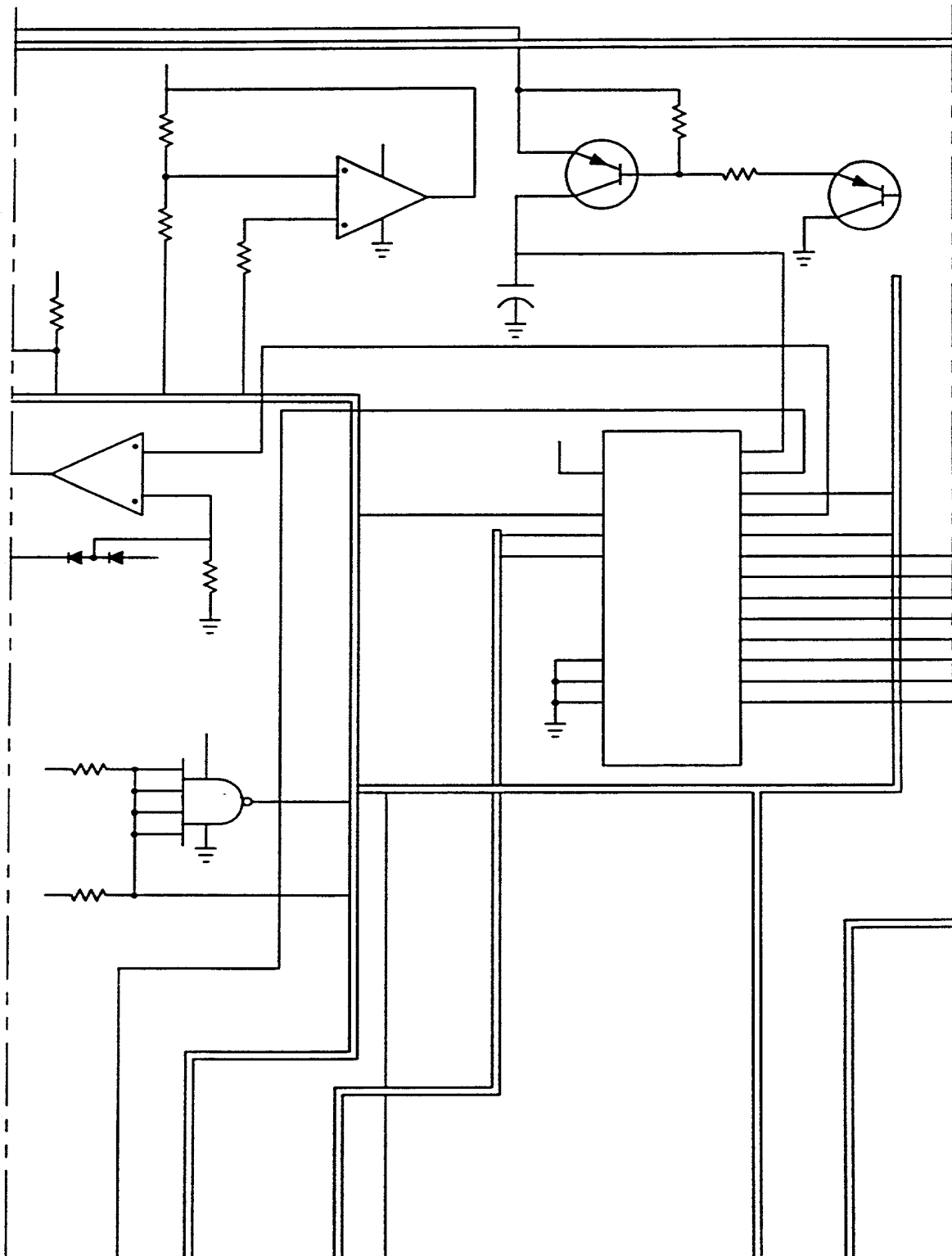


FIG. 44C

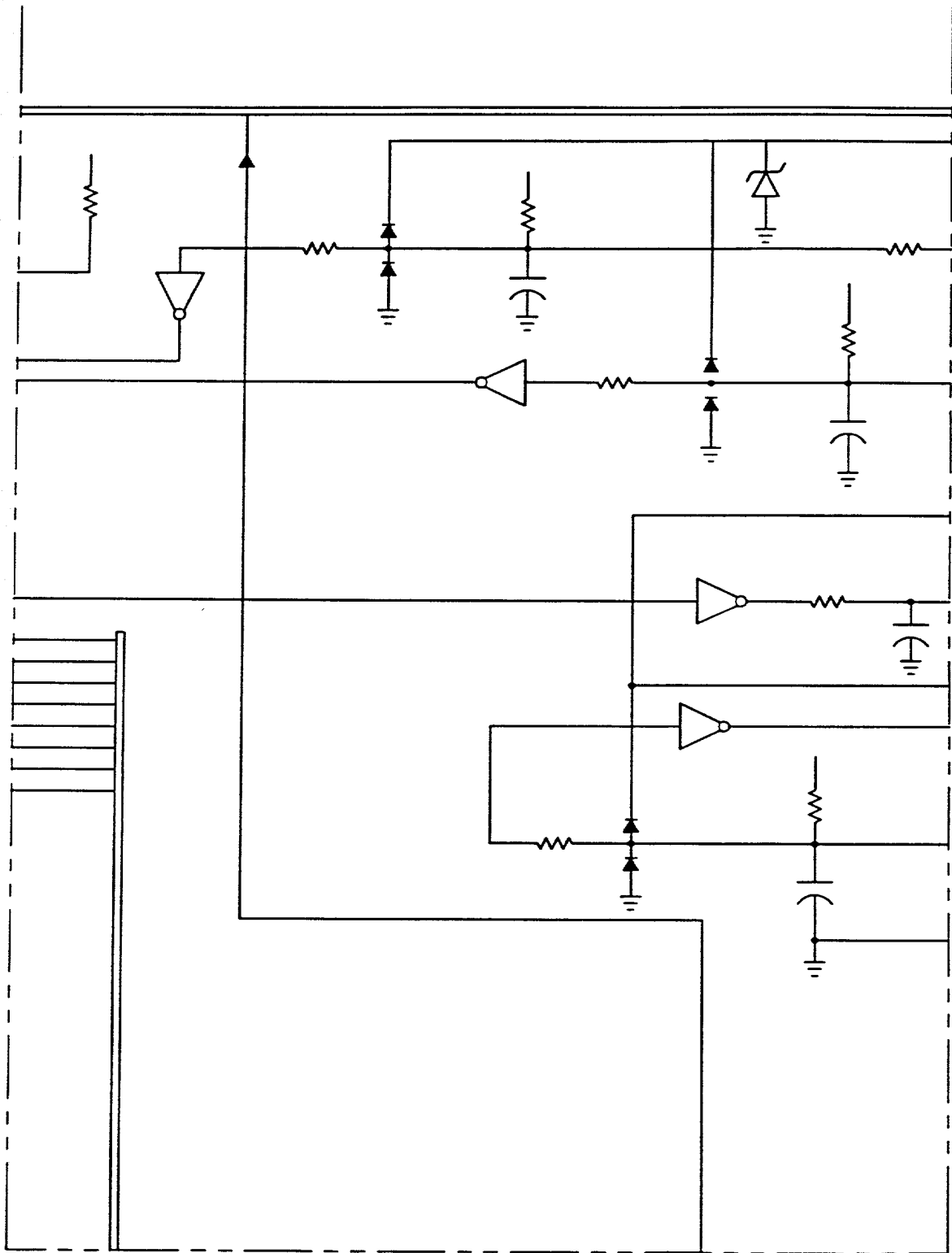


FIG. 44D

52/69

FIG. 44D is a schematic diagram of a circuit for a semiconductor device. The circuit includes a plurality of input lines, a plurality of output lines, and a plurality of control lines. The circuit is configured to receive data from the input lines and output data to the output lines, with the control lines providing control signals to the circuit. The circuit includes a plurality of transistors, resistors, and capacitors, which are connected in a manner that allows the circuit to perform the desired function.

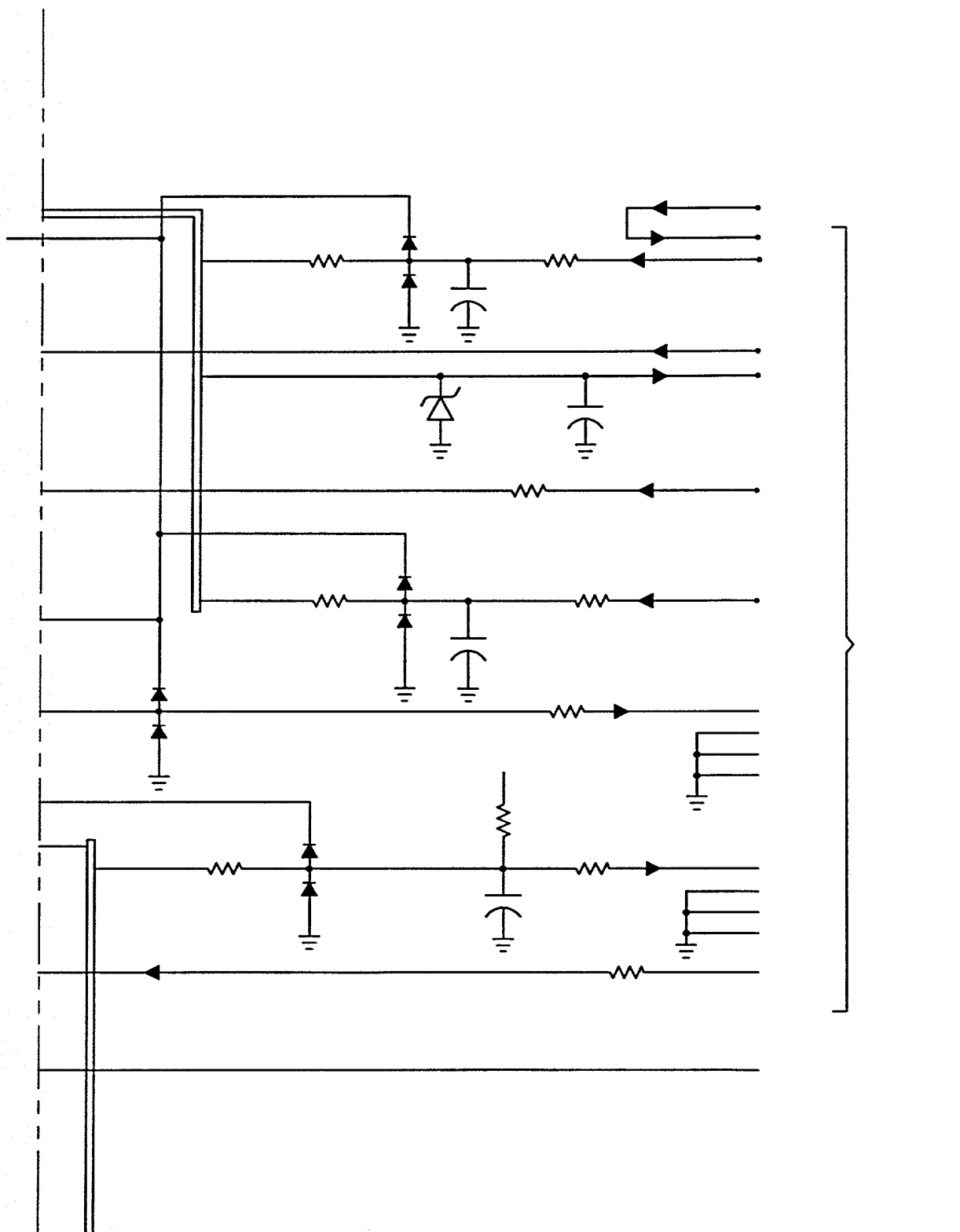


FIG. 44E

53/69

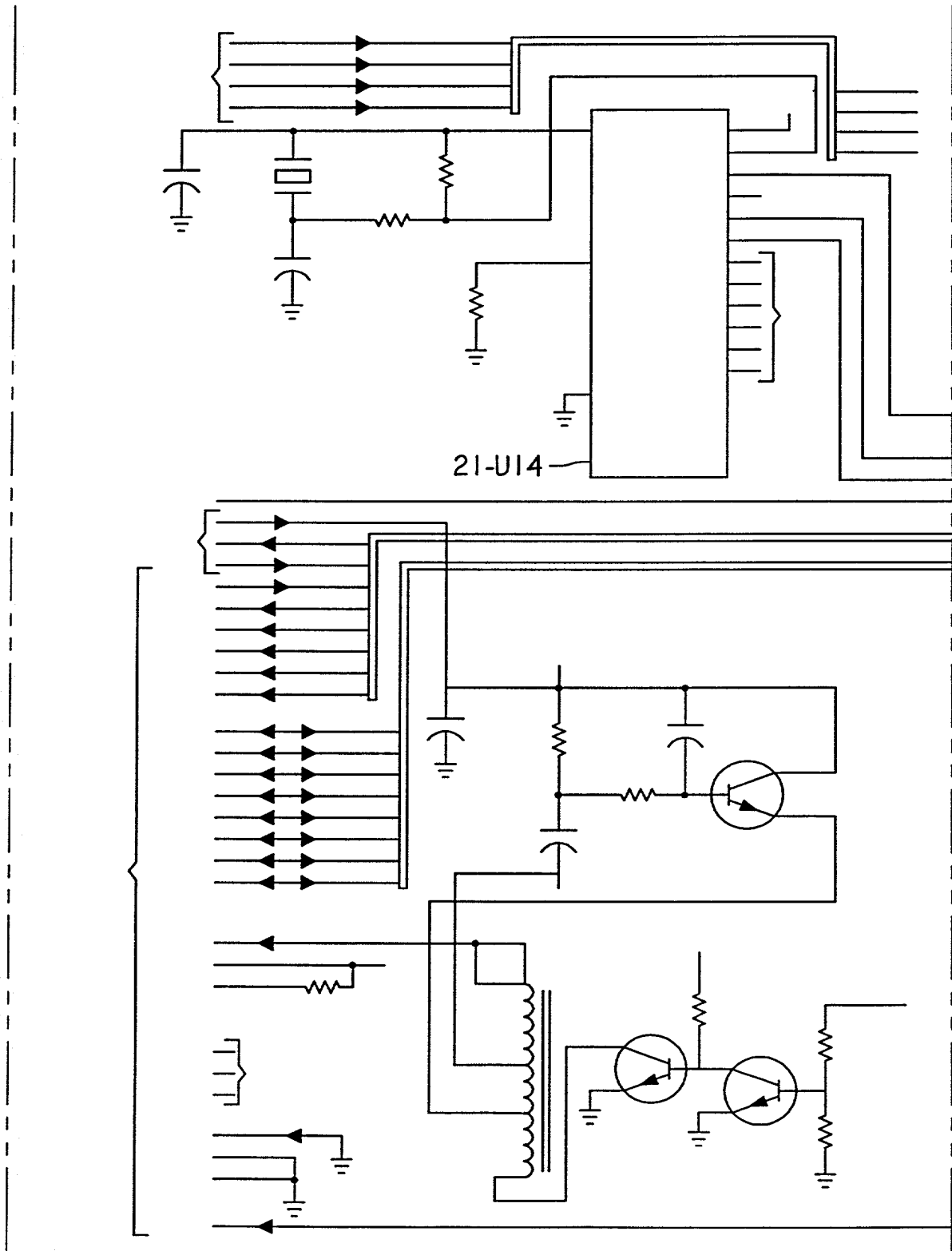


FIG. 44F

54/69

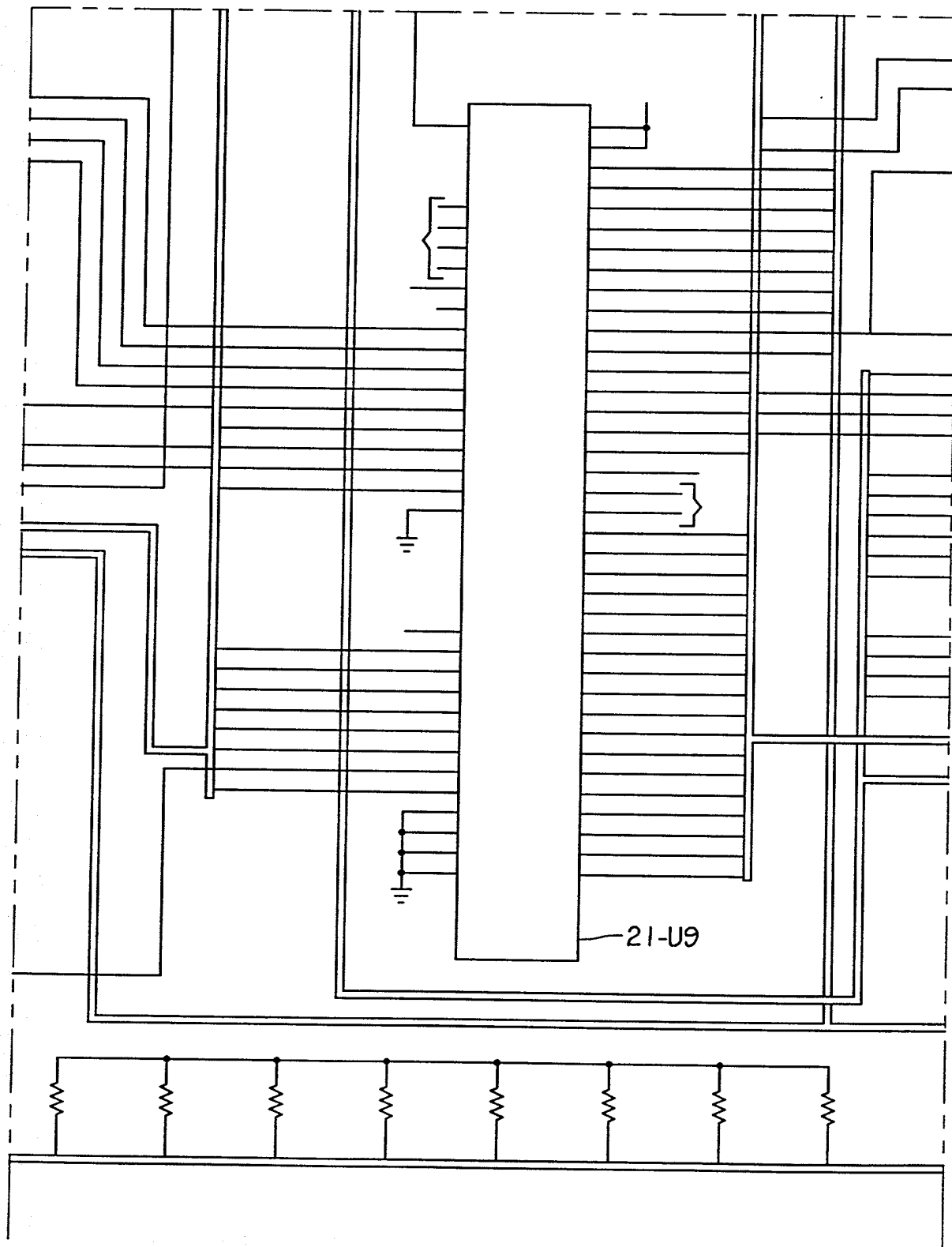
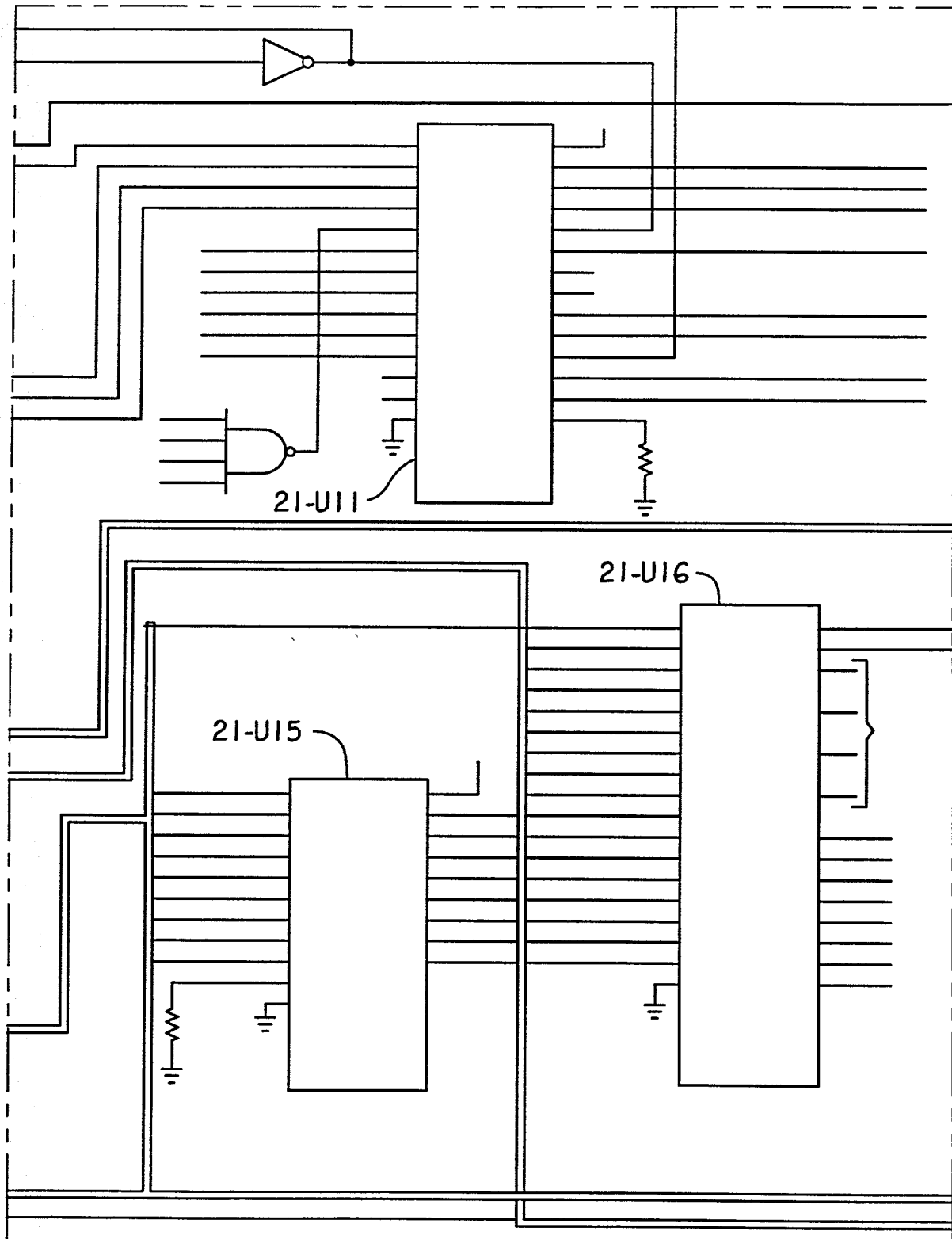


FIG. 44G



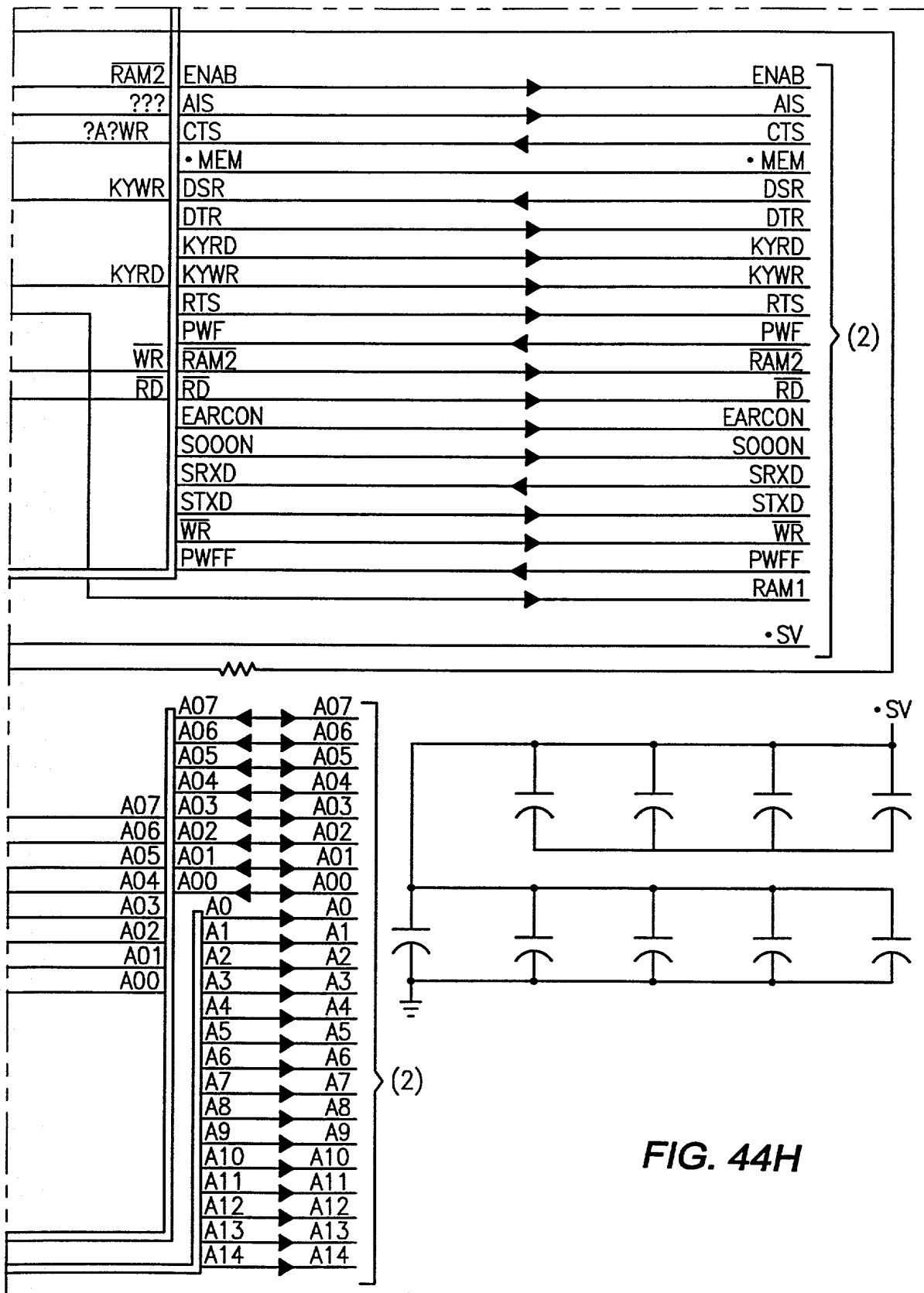


FIG. 44H



57/69

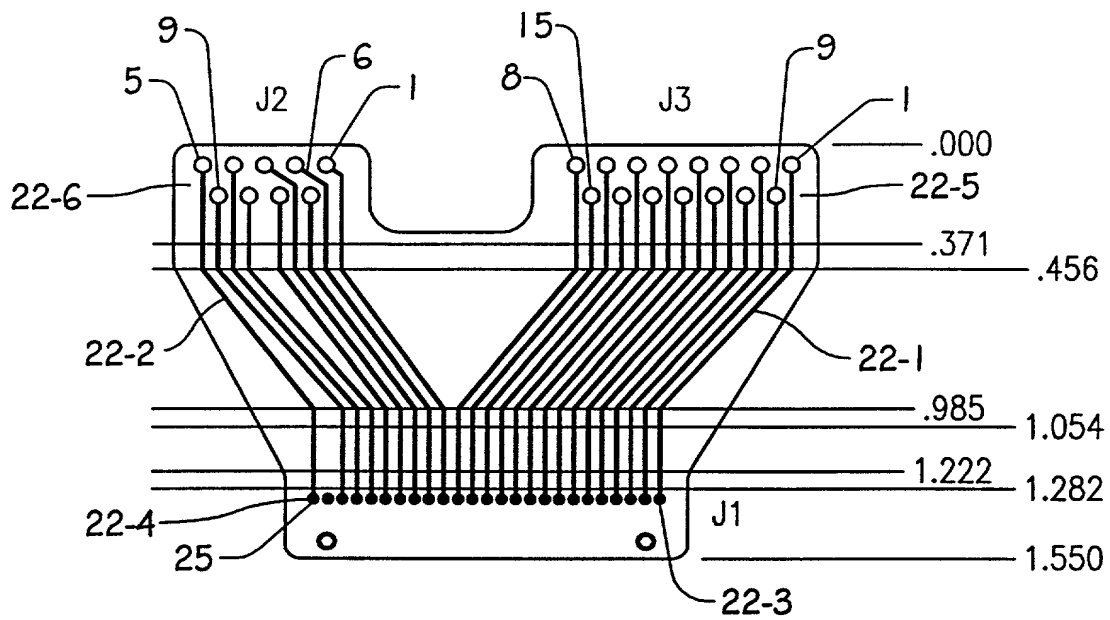


FIG. 45A

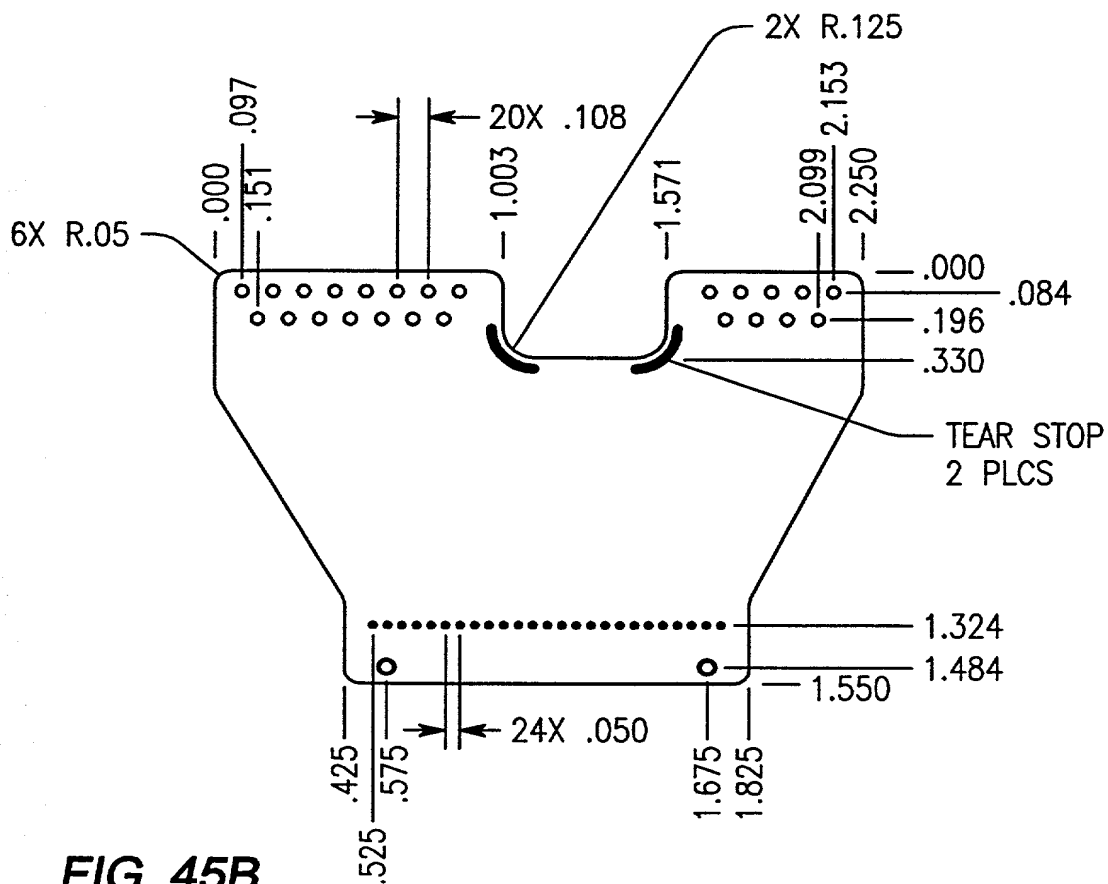


FIG. 45B

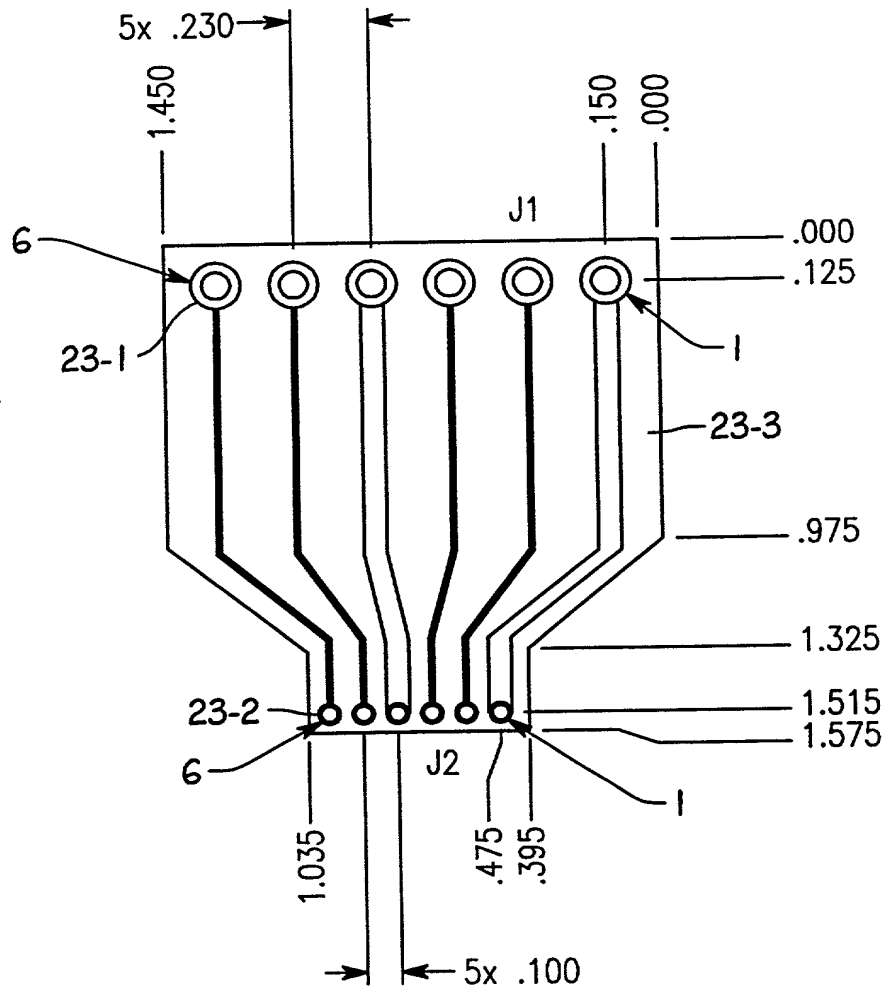


FIG. 46

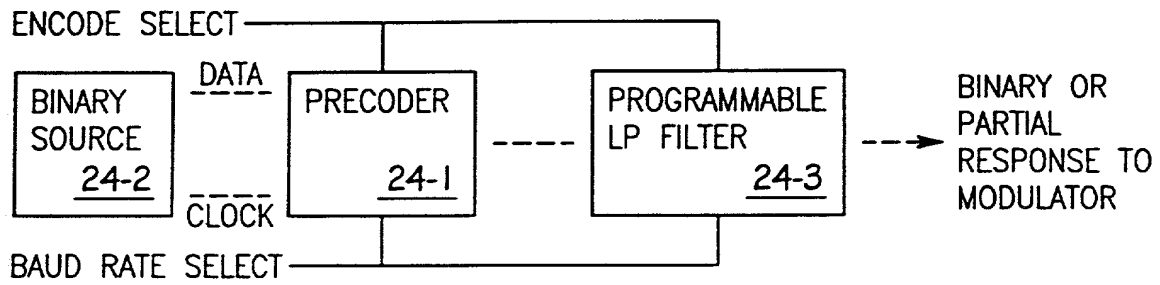


FIG. 47

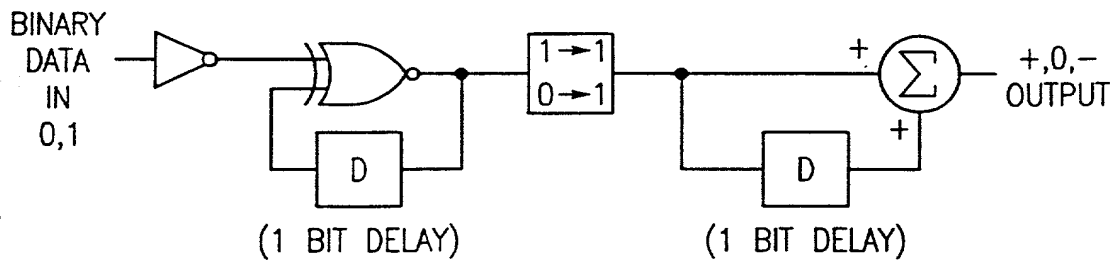


FIG. 48

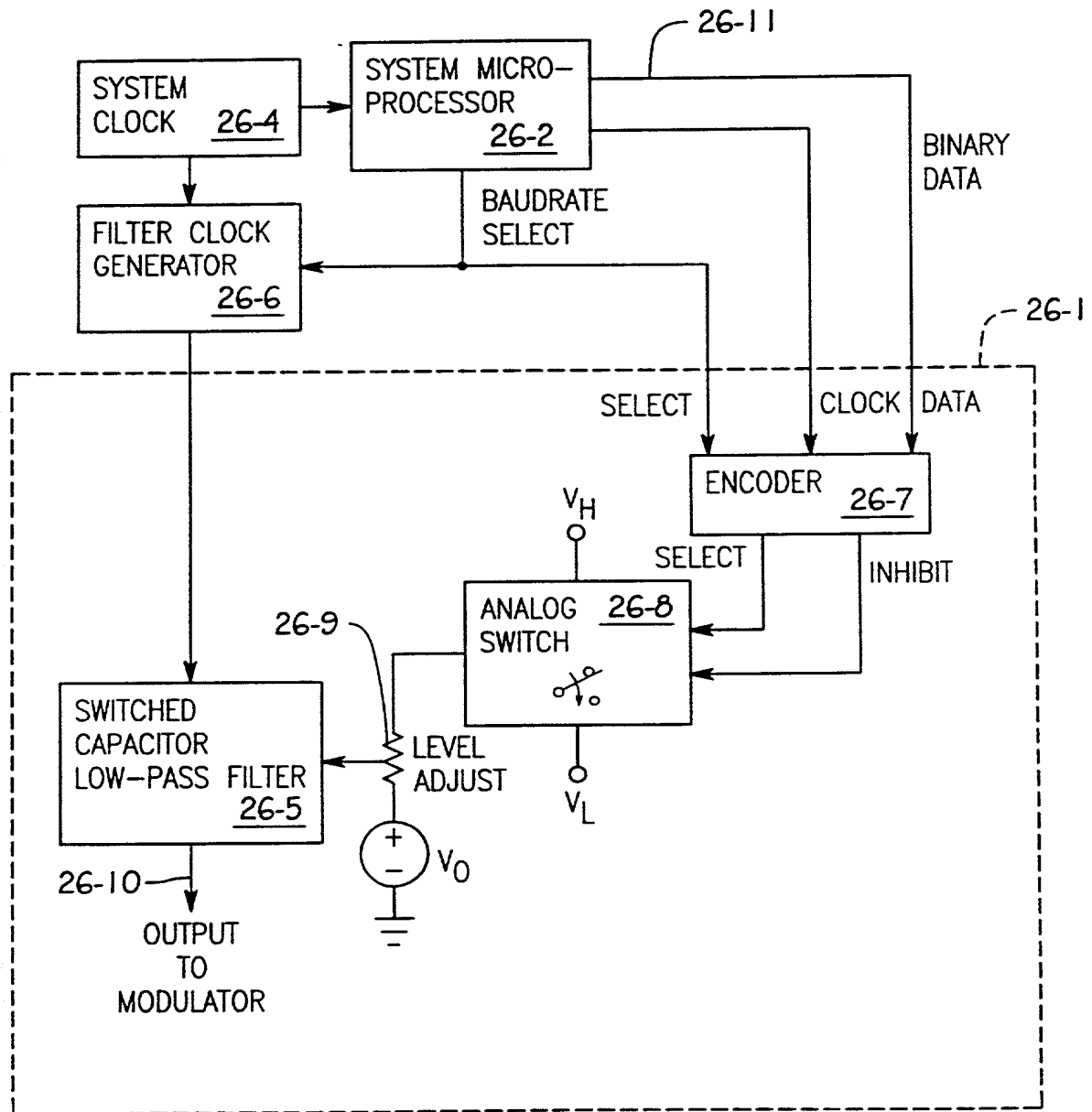


FIG. 49A

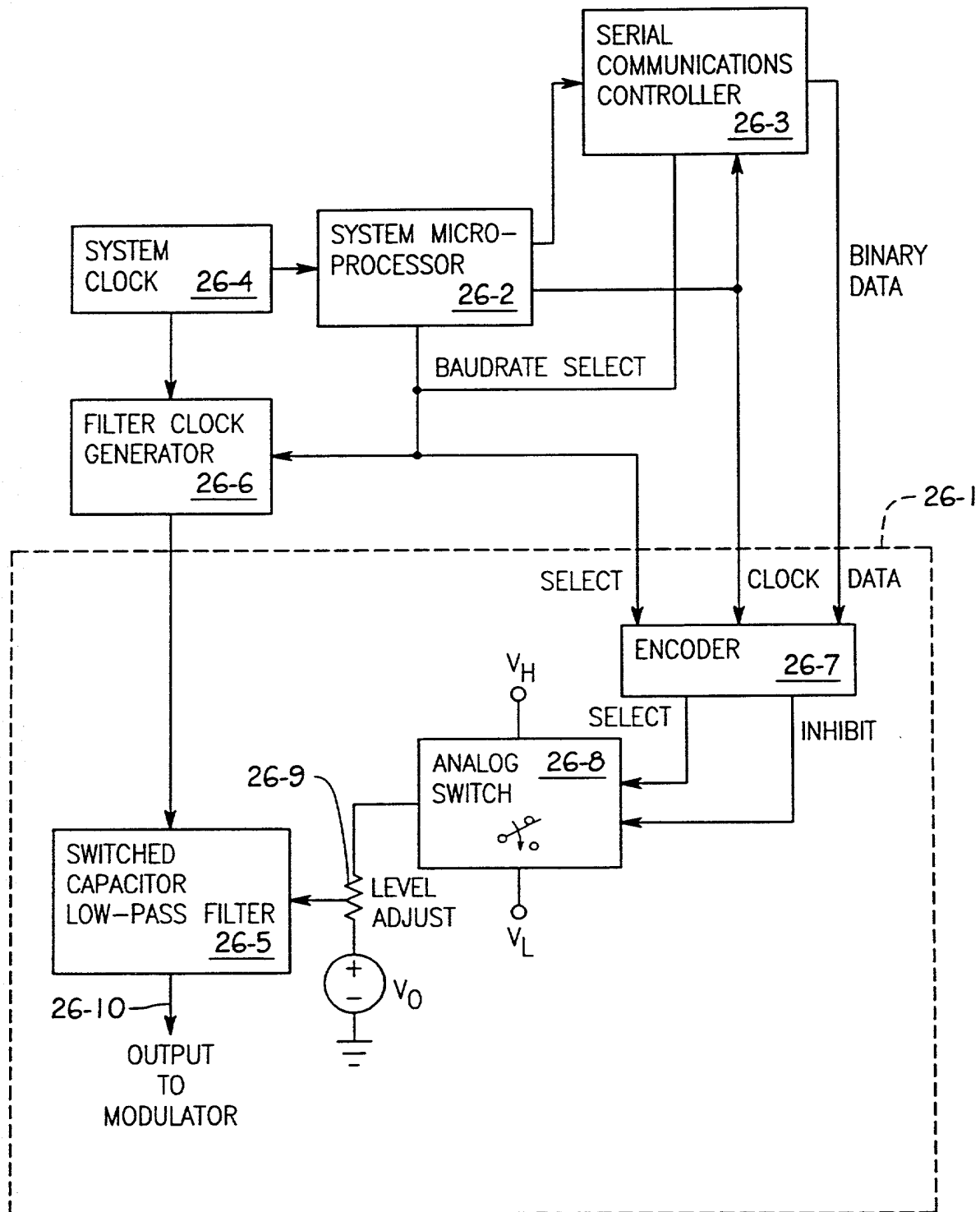


FIG. 49B

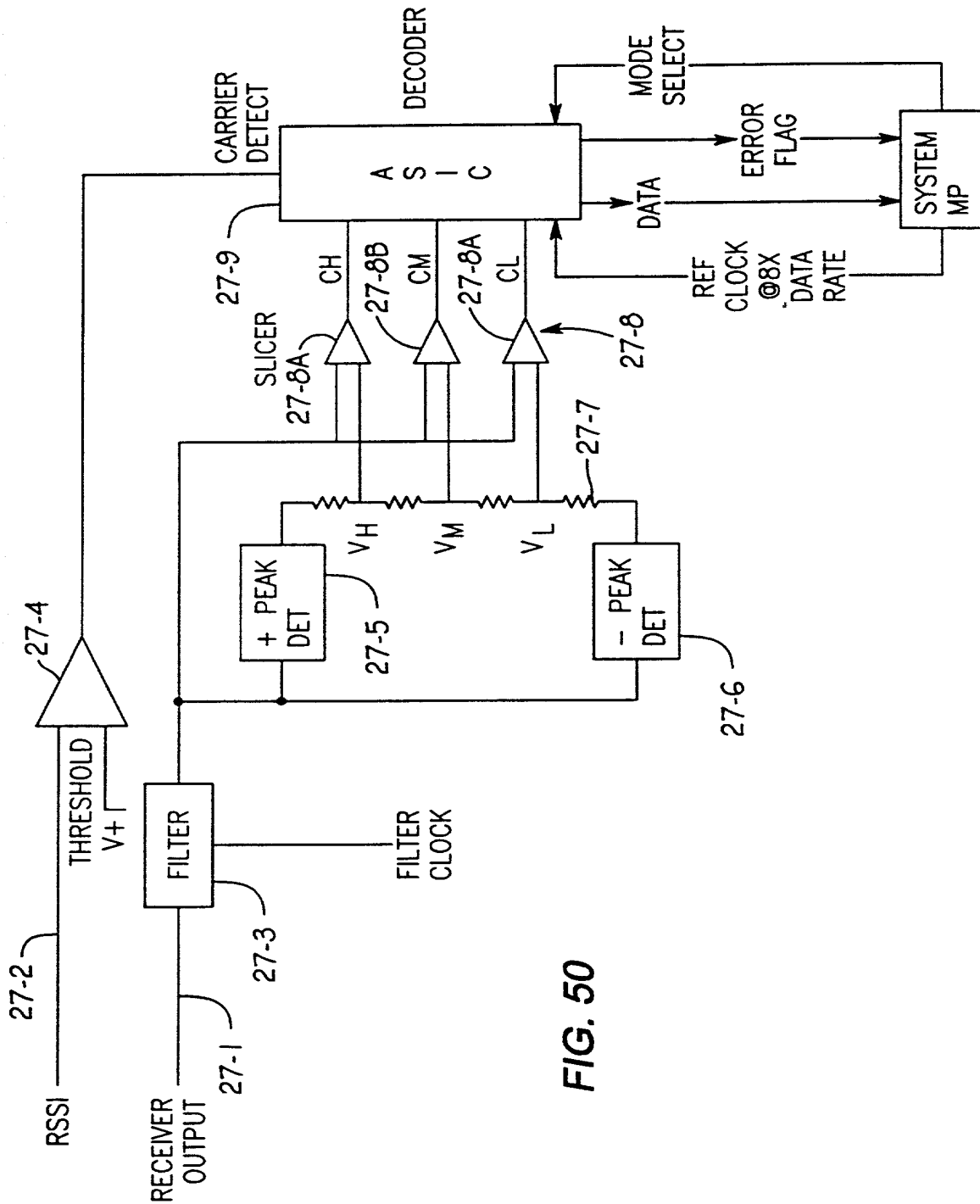


FIG. 50

FIG. 51A

TRANSMIT ???



FIG. 51B

??? DATA



FIG. 51C

SELECT



FIG. 51D

??? DELAY



FIG. 51E

TRANSMIT FILTER OUTPUT (WITH FILTER DELAY REMOVED)

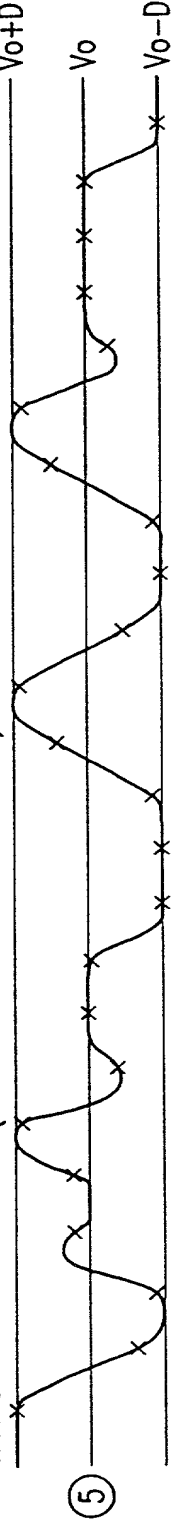


FIG. 51F

RECEIVE FILTER OUTPUT

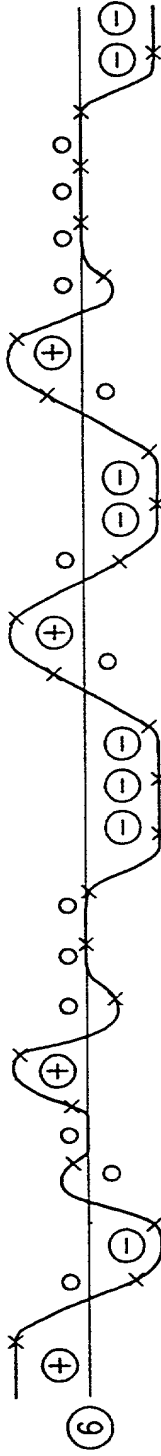
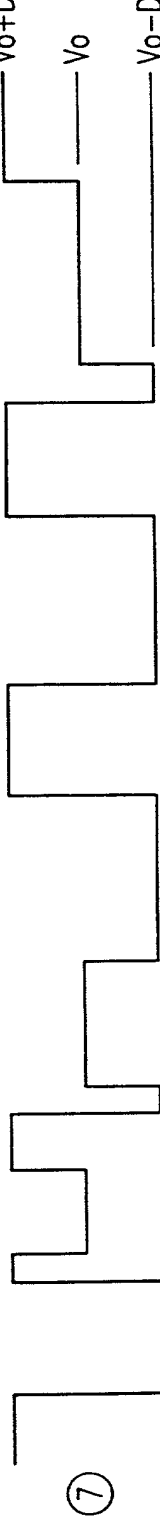


FIG. 51G

TRANSMITTER ANALOG ??? OUTPUT



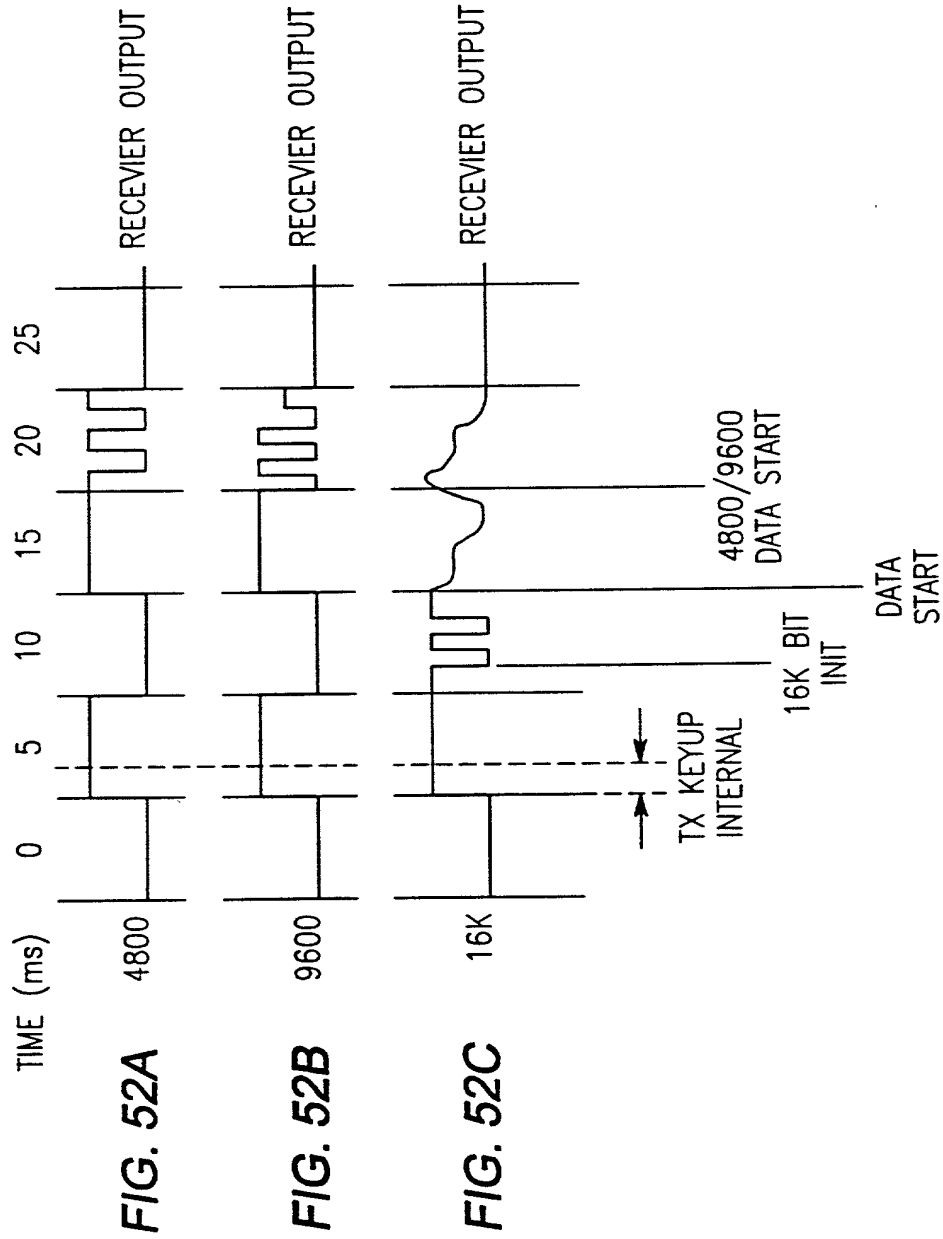
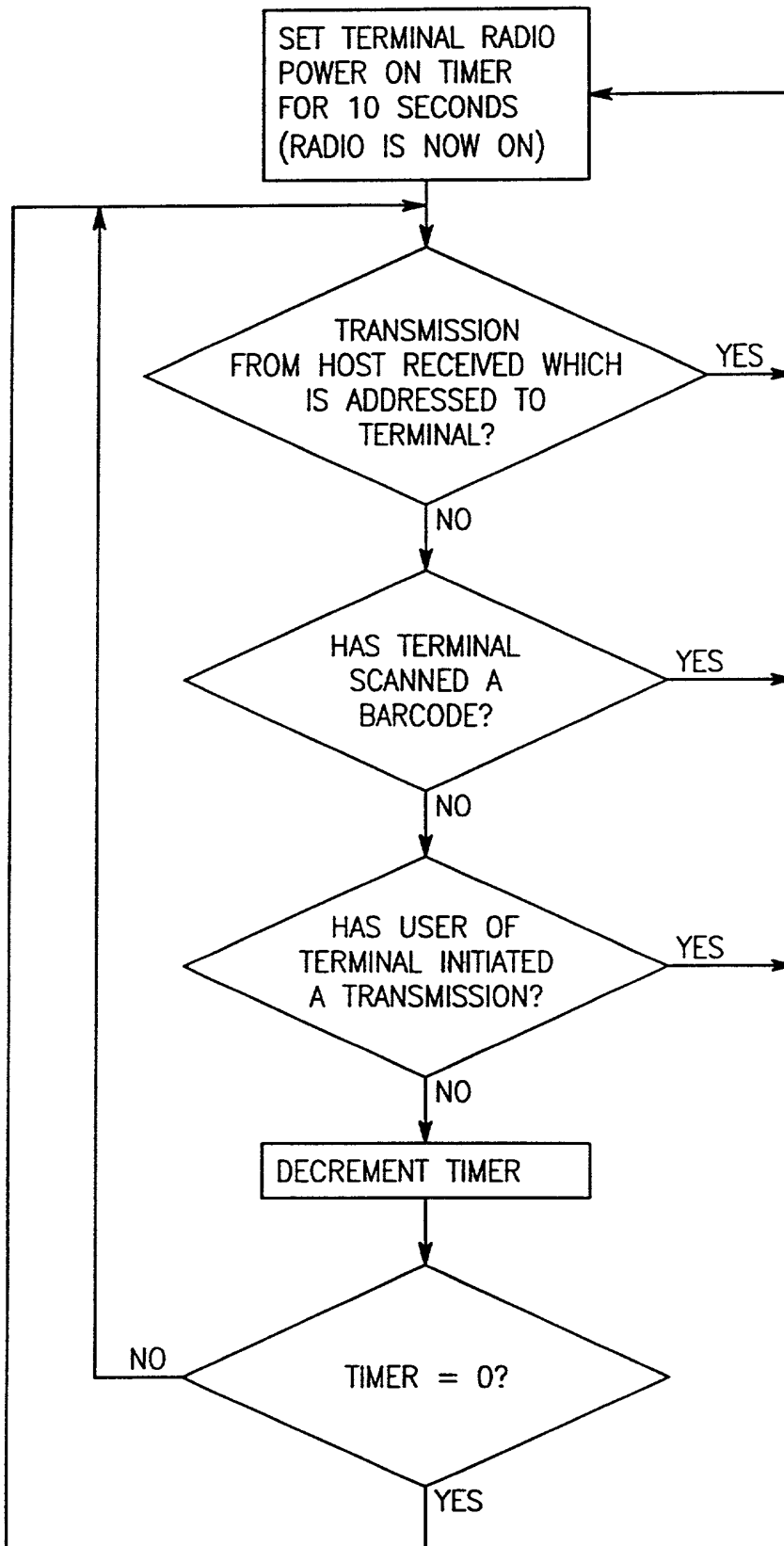




FIG.  
53AFIG.  
53B

FIG. 53A



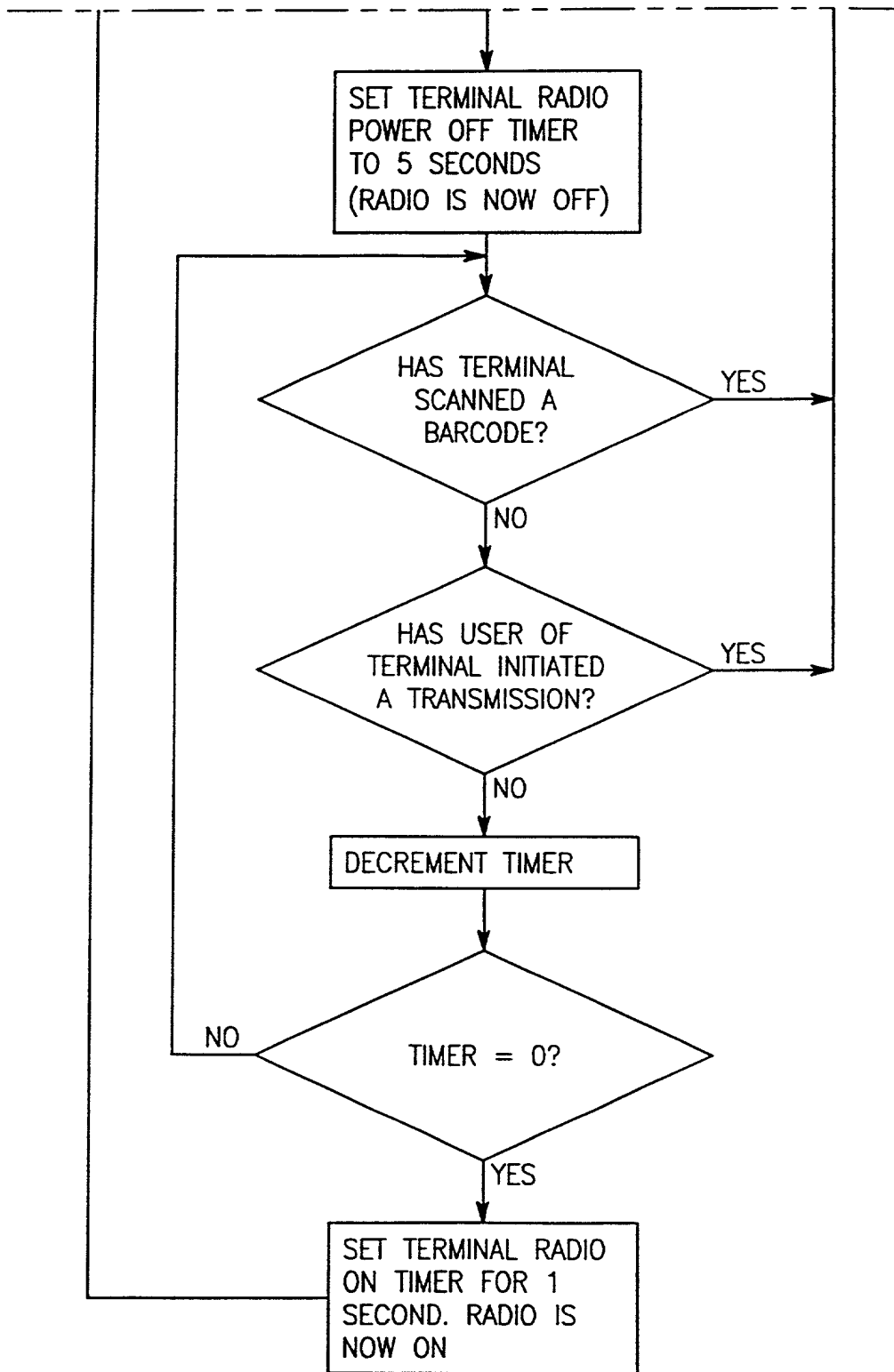


FIG. 53B

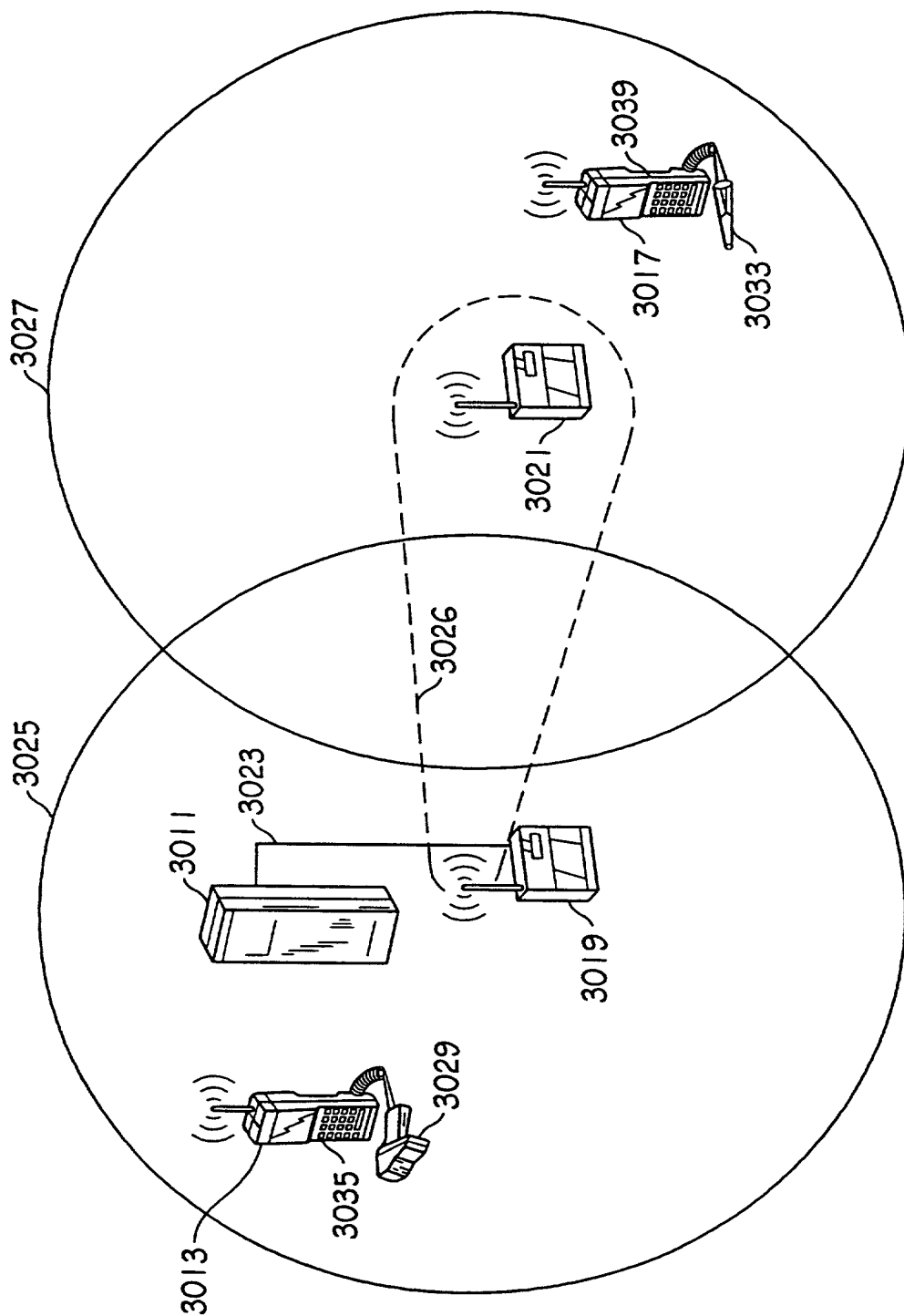


FIG. 54

FIG. 55A

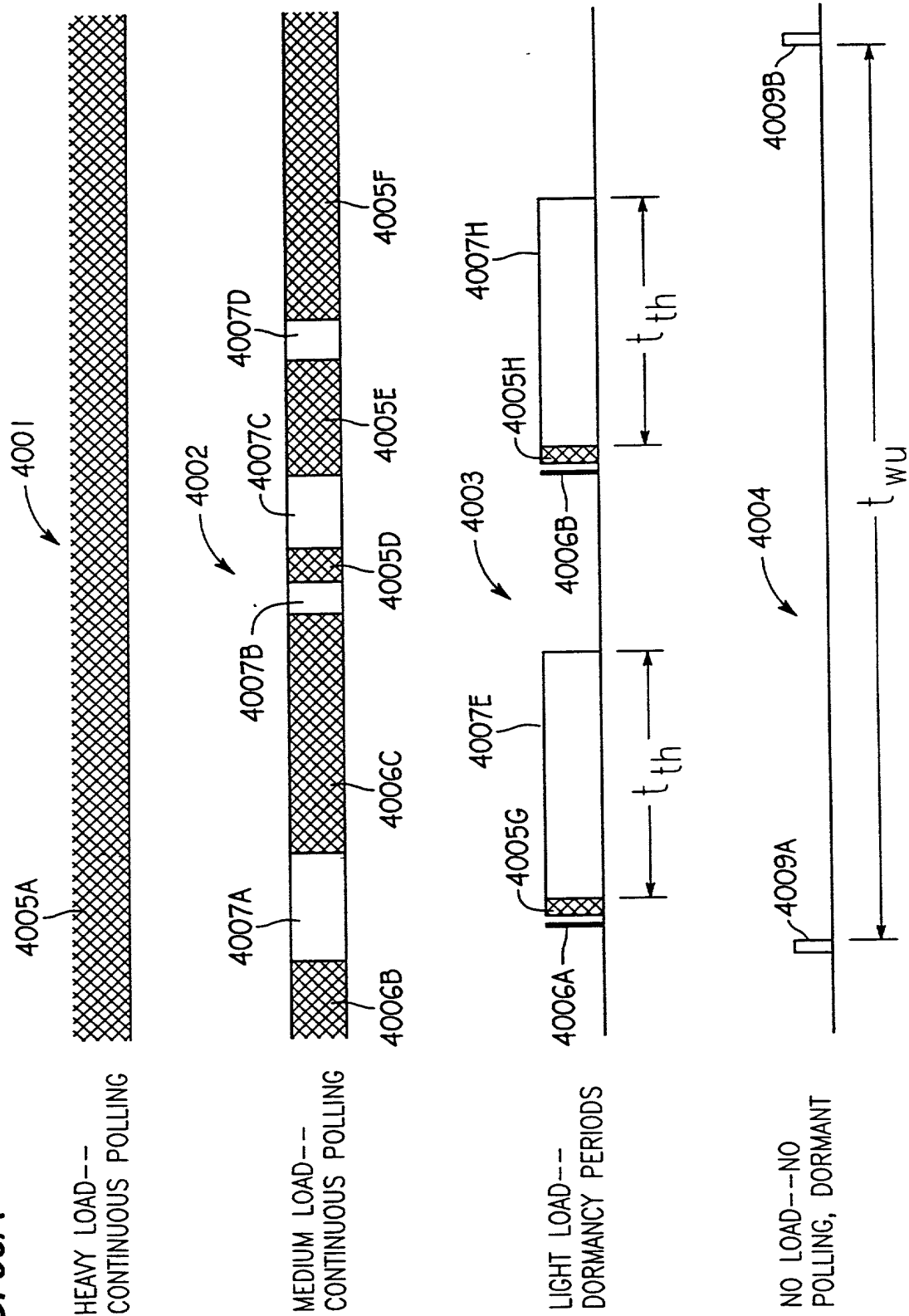


FIG. 55B

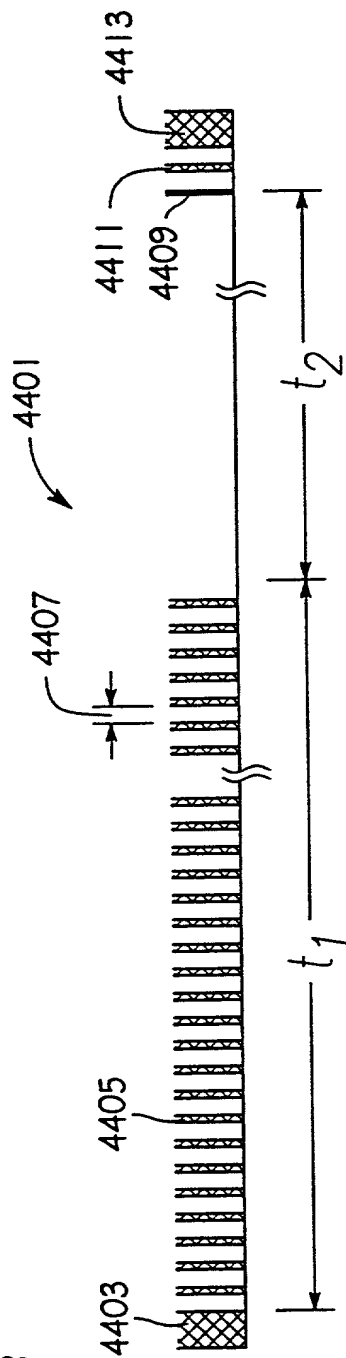


FIG. 55C

